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A Low-power Multichannel Telemetry System for High-speed Wireless Neural Recordings

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A LOW-POWER MULTICHANNEL TELEMETRY SYSTEM FOR HIGH-SPEED WIRELESS NEURAL RECORDINGS

by

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A DISSERTATION

Submitted to the faculty of the University of Alabama at Birmingham,
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Doctor of Philosophy

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A LOW-POWER MULTICHANNEL TELEMETRY SYSTEM FOR HIGH-SPEED WIRELESS NEURAL RECORDINGS

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COMPUTER ENGINEERING

ABSTRACT

The advances in microelectronics and wireless communication are going to change our lifestyles and benefit our healthcare system in the foreseeable future. New conception named "Ubiquitous Healthcare" has been proposed. It envisions a continuous, real-time, remote monitoring on the health conditions of people through the wireless communication network. Traditional biosignal monitoring devices need wire-connections for the recording, which may cause skin rupture and body infection. The physical connections also limited the number of the integrated recording channels. A low-power implantable multichannel telemetry system which can be implanted in the body and transmit recordings wirelessly can solve the problem of the traditional method. However, the design of such a low-power multichannel telemetry system is challenging. In this study, we have designed a telemetry system which possesses several merits in terms of power dissipation, system sensitivity, and data transmission rate. Research efforts have been made to address the critical design challenges of low-power consumption, high data rate communication, low cost and miniaturization, by employing subthreshold MOSFET based design, noise optimization, neuromorphic architecture and judicious use of positive and negative feedbacks. As a sensor signal acquisition unit, a low-power low-noise self-biased CMOS amplifier has been demonstrated. Modified spike detection algorithm, frequency-enhanced nonlinear energy operator (fNEO) and energy-of-derivative (ED), have been formulated and validated through CMOS all-inverter based circuit architecture. For spectrum efficient high data rate communication, a modified Hermite polynomial based ultra-wideband pulse generation schemes have been proposed and demonstrated with neuromorphic circuits.

Keywords: Analog Circuits, RF Circuits, Telemetry System, Wireless Communication.

DEDICATION

TO MY BELOVED PARENTS, WIFE, AND SON.

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First and above all, I praise God, whose blessings make me who I am today. The almighty provide me the opportunity, spirit, and capability to proceed successfully.

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1. INTRODUCTION

Background

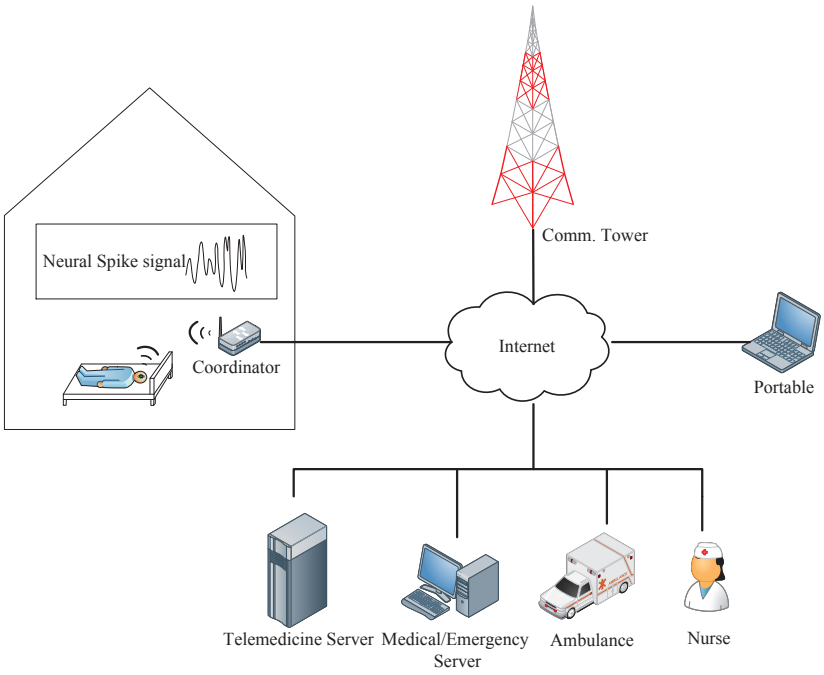
Along with the advances in microelectronics and wireless communications, a novel concept named 'ubiquitous healthcare' has been proposed nowadays. As shown in Fig. 1(a), a ubiquitous healthcare system offers doctors and nurses a more efficient way to monitor the health conditions of patients through communication network and Internet. Its telemetry attribute allows a continuous monitoring on the progression of chronic diseases, the body reaction to therapeutic drugs, and the post-operative recovery of patients. This continuous monitoring ensures a rapid response from healthcare providers when a disease outbreak occurs. In addition, the remote body inspection provided by the ubiquitous healthcare system benefits patients by saving their time and money. With the help of a ubiquitous healthcare system, the patients do not need to go to hospitals and spend about one entire day there. Instead, they only need to contact their doctors from their homes and get the inspection results rapidly, which saves the cost of transportation and the outpatient services.

A low-power multichannel telemetry system which can achieve multichannel neural recordings wirelessly is the most critical component in the healthcare system. The detection sensitivity and the transmission speed of a telemetry system determine the integrity and the fidelity of the recorded neural signals which influence the performance of the healthcare system directly. In addition, a miniaturized telemetry system can be implanted into the brain and be used to develop a brain-machine interface (BMI) for paralyzed patients. As shown in Fig. 1(b), an implantable multichannel telemetry system can control a robotic arm to move objects for disabled people. A block diagram of a typical multichannel telemetry system is drawn in Fig. 2. The system can be divided into three stages: an amplification stage, a data compression stage and a wireless transmission stages. The amplification stage usually has multiple recording channels which provide the necessitated high spatial resolution for neural signals. Among them, each channel has a biopotential amplifier which

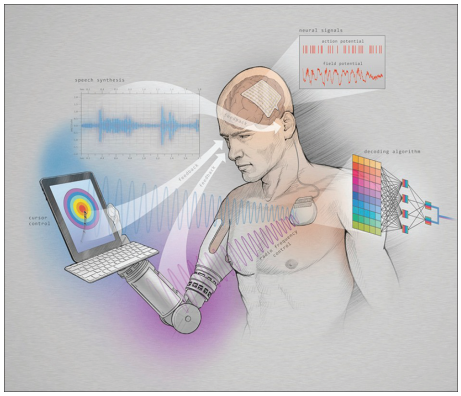
is used to amplify the target signal without introducing detectable circuit noise. The data compression stage is typically realized with a spike detector. The spike detector can identify the neural spikes from background signals and therefore removes the redundant data in the recording. By incorporating a spike detector, a telemetry system can effectively reduce the data volume and relaxes the bandwidth requirement on wireless data transmission. The last stage of a telemetry system is a wireless transmitter. This is the most important stage of a telemetry system and is also the bottleneck of high-speed neural recordings. The contradiction between power dissipation and data rate creates the principal challenge in the design of a telemetry system.

Motivation

Wireless multichannel neural recordings are very useful in today's neuroscience research, clinical diagnosis and for the development of healthcare devices. Owing to its wireless feature, a multichannel telemetry system eliminates the risks of skin rupture and body infection on subjects. By excluding the use of a large bundle of transcutaneous wires, wireless recordings offer neuroscience researchers the opportunity to investigate neuronal activities of freely behavioring animals. In addition, without the space limit caused by the physical sizes of wires, it is possible for a multichannel telemetry system to integrate more channels in a small area. As biological nerves typically have a high neuronal density, this multichannel high-density recordings provide valuable high spatial resolution information concerning the propagation of neuronal signals. For neuroscience research, this high-speed multichannel neural recordings allow neurologists to study the functionality of each neuron in a neural network. For clinical applications, high spatiotemporal resolution neuronal signals have multiple applications, such as disease prediction, medical diagnosis and drug evaluation. For advanced medical device developments, high-speed multichannel neural recordings help engineers improve the control and movement accuracy of neuroprosthetic devices. Despite having all these merits, high-speed multichannel neural recordings are



(a)



(b)

Figure 1: (a) A ubiquitous healthcare system. (b) An implantable multichannel telemetry system used for BMI robotic arm control. (Picture is from Nathan C. Rowland, etc. 2013 [**1**])

difficult to be obtained due to the challenges in the design of a low-power multichannel telemetry system.

The development of a low-power multichannel telemetry system for high-speed wireless neural recordings are challenging in multiple technical aspects. The most important one is the power dissipation of the system. Since a heat flux of 80 mW/cm^2 can cause the

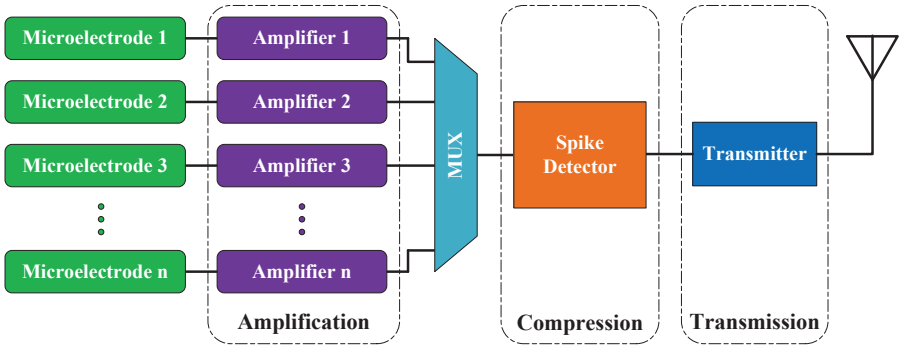


Figure 2: The block diagram of a multichannel telemetry system. MUX: multiplexer.

necrosis of surrounding tissues [**2**][**3**], a low-power design which means low tissue heating is mandatory for the purpose of safety. As the increase of recording channels, the power budget assigned to each recording channel is further reduced. In addition, low power dissipation guarantee a chronic use of devices without frequent battery recharging or energy harvesting. A lower power dissipation allows the use of a smaller battery that makes small-size and light-weight system possible. In account of these challenges, minimizing power dissipation of the system should be the priority in the design. The second challenge is the detection sensitivity of the system. Since neural signals [**4**] are typically in the range of 10 $\sim$ 500 μV with a noise level of 5 $\sim$ 10 μV_{rms}, a low-noise high-gain amplification stage [**2**] is required for high sensitivity detection. A study on low-power low-noise amplifiers is important for the development of the system. The third challenge is the transmission data rate. The increase on the number of channels causes a growth on data volume resulting in a significant problem for wireless data transmissions. For instance, if a system has 128 channels and each channel has 8-bit resolution at the Nyquist sampling rate requires 20 Mb/s data rate, the target signal is 10 kHz [**5**]. As the number of channels increases, the data rate will reach 100 Mb/s and even higher [**6**]. To achieve this data rate, a data compression stage and a high-speed wireless transmission stage are needed in the system. However, both of them must be designed under a constraint power budget. Last but not least, a system-on-chip (SoC) architecture is preferred in most of the design, which prevents the use of large capacitors and inductors.

2. LITERATURE REVIEW

In order to achieve all the functions with the minimum power dissipation, pioneering researchers have made great efforts on the design of biopotential amplifiers, spike detectors, and wireless transmitters.

A biopotential amplifier [**2**]-[**7**] which acts as the first amplification stage is one of the most important components in an implantable neural recording microsystem. The performance of a biopotential amplifier determines the complexity of the post signal processing. A well-designed low-power low-noise amplifier can improve the system sensitivity, dynamic range and power-efficiency. In the recent years, multiple high performance biopotential amplifiers [**4**]-[**13**] have been reported by pioneering researchers. Some of the research groups [**4**],[**13**] have designed the biopotential amplifier with input-referred noise values in the range of $2 \sim 4\ \mu V_{rms}$, but the power dissipation is usually larger than 10 μW. On the other side, some of the studies have developed amplifiers [**9**] with microwatt or sub-microwatt power dissipation, but the input-referred noise values are generally above 10 μV_{rms}. However, as the advances of neurobiology, high-sensitivity high-precision recordings have become a mandatory. It requires the design of amplifiers with $\sim 2\ \mu V_{rms}$ input-referred noise while dissipating only a few microwatt power. To strike a balance on the noise performance and power dissipation, a numeric value called noise efficiency factor (NEF) [**2**] has been widely used by the researchers to evaluate the power-noise efficiency of their designs. A smaller NEF value indicates a higher power-noise efficiency which is preferred for a design.

A carefully designed spike detector can effectively reduce the power dissipation of a microsystem by minimizing the transmission data. Given the low occurrence rate of neural action potentials (APs), about 10 to 120 occurrences per second, it is promising to achieve a great data compression by removing the redundant data at the intervals of spikes. Although

a spike detector itself may dissipate some extra power, but comparing with the power reduction brought by the data compression, up to 5 times as reported [**14**], introducing a low-power spike detector is till an energy-efficiency policy. A spike detection algorithm is the core of a spike detector. A variety of mathematical tools have been employed for the studies of the spike detection algorithms, such as thresholding [**15**], spike derivatives [**16**], and energy operators [**17**]. Because of its low computation complexity, robust and unsupervised features, the nonlinear energy operator (NEO) [**17**]-[**20**] has become the mostly used spike detection method. The low power implementations of NEO spike detectors have been extensively reported in the past years. Based on the sub-threshold design, a NEO spike detector [**18**] achieves a power dissipation of 2.7 μW. Another study [**19**] combining the NEO spike detector and the spike feature extractor together dissipates only 1 μW power. A NEO spike detector [**20**] which improves the detected waveform integrity has achieved a power dissipation as low as 780 nW. However, these studies only target on the noise degraded spike signals and fails to address the impact of large-amplitude baseline disturbance on the spike detections. This disturbance that is a mixture of local field potential (LFPs) and APs from neighbouring neurons may have an amplitude as high as 1 mV with frequency content up to 200 Hz [**21**]. Since LFPs contain valuable information for the clinic applications, such as epileptic seizure [**22**], it is highly desirable to investigate a robust method for the spike detection at the presence of the LFP.

In wireless data acquisitions, the advances in micro-electromechanical systems (MEMS) have made it possible to integrate more recording channels in a small area. However, this increase on the number of channels causes a growth on data volume resulting in a challenge for wireless data transmissions. For example, a 128-channel recording system with 8-bit resolution at the Nyquist sampling rate requires 20 Mb/s data rate when the target signal is 10 kHz [**5**]. As the number of channels increases, the data rate reaches 100 Mb/s and higher [**6**]. Impulse radio based ultra-wideband (IR-UWB) communication can be a excellent strategy for high-speed neural recordings [**5**][**6**]. Sub-GHz UWB communications occupy a lower band (0 - 960 MHz) [**23**] than the standard UWB communications (3.1 -

10.6 GHz). The relatively lower frequency spectrum relaxes the system requirements on the circuit design and the communication synchronization, which ultimately reduces total power dissipation of the system. In addition, the sub-GHz UWB pulses have been proven to hold low attenuation in air, good penetration and little group delay [**23**][**24**].

2.0.1. *Research Approaches*

In this study, we have employed the approach of application-specific integrated circuits (ASIC) design which customizes the circuit based on the requirements of the system. A carefully designed ASIC system uses the minimum power to achieve all functionalities. For amplification stage, we have utilized CMOS weak inversion design to achieve an ultra low-power low-noise signal amplification. For data compression stage, NEO based spike detection method has been studied to implement an ultra low-power spike detection. For data transmission stage, we have investigated the sub-GHz UWB transmitter. Through an in-depth study on the mathematical model of pulse generations, a low-power pulse generator has been investigated for sub-GHz UWB communications.

2.1. Specific Aims

The objective of this dissertation is to develop a low-power multichannel telemetry system for high-speed wireless neural recordings. In order to achieve this goal, we have demonstrated three subsystems with a 0.13-μm CMOS process: a low-power low-noise biopotential amplifier, an ultra-low-power high sensitivity spike detector and a power-efficient pulse generator. The three specific aims are described as follows:

2.1.1. *Aim 1: Development of a low-power low-noise biopotential amplifier for signal amplification*

For identical overall power dissipation, the increase of channel numbers shrinks the power budget assigned to each biopotential amplifier, because each channel requires one amplifier.

On the other hand, as neural signals are typically in the range of $10 \sim 500\ \mu$V with a noise level of $5 \sim 10\ \mu V_{rms}$ [**2**], a low-noise amplification is desired in practical applications. The aim of this work is to customize an amplifier which holds an optimized performance on power dissipation, device noise, and voltage gain for neural signal amplifications. To achieve this aim, we have employed the subthreshold CMOS circuit design to achieve a maximized power efficiency (g_m/I_D). Two specific amplifiers have been studied. The first one is targeted to the application requiring very-large-scale neural recordings which generally demands the number of recording channels up to 1000. For this application, a biopotential amplifier needs to achieve an extremely low power dissipation ($\sim$100 nW). The second amplifier is target on low-noise performance which is critical for high-sensitivity neural recordings. A gain-tunable feature have been investigated in this amplifier to fully explore the resolution of analog-to-digital (ADC) block.

2.1.2. *Aim 2: Development of a low-power high-sensitivity spike detector for data compression*

Data compression stage is required due to the large data volume caused by the increase of recording channels. Neural spike detectors can effectively reduce the total power dissipation of the system by minimizing the transmission data. The aim of this work is to develop a spike detector to achieve a continuous high-sensitivity spike detection. To achieve this goal, two specific tasks must be completed. The first one is the investigation of spike detection algorithms. An efficient spike detection algorithm can enhance the detection sensitivity and lowers the power dissipation of a spike detector. The second task is to implement the proposed algorithm into a low-power high-sensitivity spike detector.

2.1.3. *Aim 3: Development of a power-efficient pulse generator for data transmission*

A pulse generator is the most important component for a UWB transmitter. The aim of this work is to develop a power-efficient pulse generator for high-speed wireless neural recordings. The strategy is to develop an orthogonal pulse based sub-GHz UWB transmitter that can achieve a high data rate (up to 100 MHz) with pure pulse shape modulation. However, the design of an orthogonal pulse generator is complicated in both mathematical modelling and circuit implementation, which may result in a very high power dissipation and cannot be used for a neural recording system. In this study, we have made a balance on the power dissipation and data rate, and proposed a power-efficient orthogonal pulse set generator.

3. BIOSIGNAL AMPLIFIERS

An Ultra-Low-Power Bioamplifier

Power dissipation of bioamplifiers has become one of the most critical factors for up-to-date implantable neural recording microsystems as the increasing of recording channels. This study presents an ultra-low-power bioamplifier [**25**] which is designed for the very-large-scale integration of neural recordings. To reduce the power, the proposed bioamplifier is designed to work with a 0.5 V power supply and all MOSFETs operate at weak inversion region. Both folded-cascode and wide-swing structures are employed to fully exploit the output swing. By producing a 18:1 bias current ratio between input transistors and load current mirror, the noise performance of the proposed bioamplifier is optimized for the given power dissipation. Designed in a 0.13-μm CMOS process, the proposed bioamplifier consumes only 61.7 nW power to obtain a gain of 23.8 dB and a bandwidth of 3.6 kHz. The input-referred noise over the entire bandwidth is 12.7 μV_{rms}, corresponding to a noise-efficiency factor of 3.1.

Introduction of Ultra-Low-Power Bioamplifier

Access to simultaneously recorded bioelectrical activities from a large number of recording sites facilitates a more accurate diagnosis of the malfunctions in human body. Multielectrode biopotential recordings using an array of microelectrodes have become a standard practice in neuroscience research [**2**]. Implantable neural recording systems enable *in situ* recording of simultaneous neural activities [**26**]. A fully implantable neural recording system must be small enough for the convenience of implantation, while its power consumption must be low enough for the length of device lifetime and also for the safety of surrounding tissues.

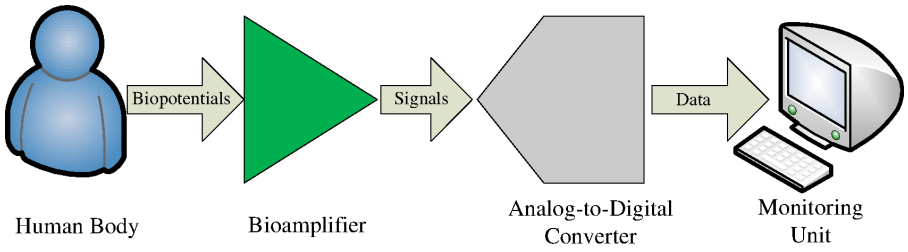


Figure 3: Biopotential recording system.

A bioamplifier is the most important component for a multielectrode biopotential recording system in terms of functionality. It is also a critical factor dictating the size and power dissipation of the system. A typical biological signal monitoring system is shown in Fig. 3. The bioamplifier needs to amplify biosignals in the range 10 μV - 500 μV with noise level of 5 μV_{rms} - 10 μV_{rms}. The characteristics of typical biosignals are shown in Fig. 4. Therefore, a high gain amplifier with a high signal-to-noise ratio (SNR) is desirable. Besides, since a heat flux of 80 mW/cm^2 can cause necrosis in muscle tissue [**2**], for an array of 512-electrodes, power dissipation must be less than 1 μW per channel for a small chip area [**9**]. All these constraints must be considered while designing a bioamplifier.

The design of bioamplifiers has attracted the interest of multiple research groups in the past decades. Harrison *et al.* have reported a bioamplifier designed in 1.5-μm CMOS process with a power dissipation of 80 μW and a noise-efficiency factor (NEF) of 4 [**2**]. A sub-microwatt low-noise amplifier [**7**] is designed for neural recording consuming only 805 nW. Kim *et al.* have proposed a 220 nW neural amplifier [**9**] with an NEF of 2.47. Most of the reported studies consume μW level power with a few exceptions. However, the high power consumption hinders the accommodation of larger number of recording channels in an implantable system. For an energy-harvested system, the power budget become even more stringent to meet the noise efficiency while supporting higher number of channels. In an effort to reduce the power consumption of an implantable bioamplifier while maintaining desirable noise efficiency factor, our group is focusing on the design of an ultra-low-power bioamplifier which can eventually support large array neural signal recording.

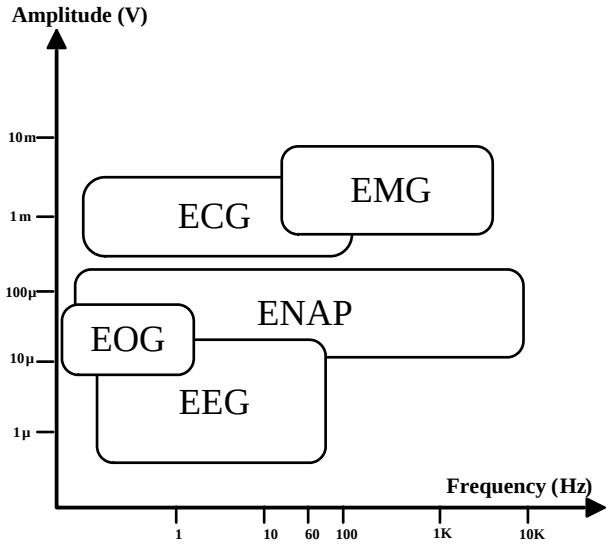


Figure 4: Characteristics of typical biosignals.

In this work, we propose a power and noise efficient bioamplifier for large array biopotential recording systems. The proposed bioamplifier utilizes a differential folded-cascode gain stage and a common-gate gain stage to amplify the biological signal. The wide-swing-cascode structure is employed to achieve high gain under low-voltage low-power operation. Subthreshold region operation of MOSFETs are utilized and the corresponding device dimensions are optimized by extensive computer simulations. The optimum trade-off of power, noise and device dimensions results in an ultra-low-power biosignal amplifier. The proposed bioamplifier is designed using 0.13-μm standard CMOS process. Monte Carlo simulation is performed to validate the system performance with respect to device dimension mismatch. Finally, a pre-recorded human electroencephalography (EEG) signal is used to confirm the performance of the proposed bioamplifier.

Proposed Ultra-low-power Bioamplifier

A high-pass filter shown in Fig. 5(a) is applied before the proposed bioamplifier to block the DC-offset which is produced by the skin-electrode interface. The core circuit of the proposed bioamplifier is shown in Fig. 5(b). The folded-cascode structures consisting

of MOSFETs operating in weak-inversion-saturation and deep-weak-inversion regions is utilized in the proposed architecture to achieve high gain with low-power consumption.

The NMOS differential pair (M_5, M_6) working in the weak-inversion-saturation acts as the first gain stage of the proposed bioamplifier. The gate terminals of M_5 and M_6, *Vin+* and *Vin-*, are the differential inputs. NFETs are selected here instead of PFETs to ensure a high transconductance which is important for the noise suppression. The primary challenge of designing a bioamplifier is the use of constraint power budget to achieve a low-noise performance and decent signal gain. A bias current ratio of 18:1 is achieved on the drain current of transistor M_5 and the drain current of transistor M_{10}. The large bias current on the input NMOS pair produces large transconductances of M_5 and M_6 which yield a high gain on the first stage and reduce the input-referred noise of the bioamplifier.

The gain function of the input NMOS differential block can be given by

$$G_1 = -g_{m5} \cdot \left[r_{o8} || \frac{1}{g_{m10}} \left(1 + \frac{g_{m12} r_{o12} r_{o14}}{r_{o10}} \right) || r_{o5} \right] \tag{3.1}$$

where G_1, g_m and r_o represent the gain of the NMOS input differential block, the transconductance and the output resistance of the MOSFET, respectively. The output signals then pass through the common-gate gain stages (M_9, M_{10}) and the gain of these stages can be represented as

$$G_2 = g_{m10} \cdot (r_{o10} || g_{m12} r_{o12} r_{o14}) \tag{3.2}$$

where g_{m10} represents the transconductance of M_{10}. Finally, the total gain of the entire bioamplifier is

$$G = G_1 G_2 \tag{3.3}$$

where G_1 and G_2 are given by (3.1) and (3.2), respectively.

Noise analysis on the proposed bioamplifier

As the design is aimed to amplify neural signals, the proposed amplifier must holds a noise performance that is good enough to process micro-volts level signals. The amplitude of

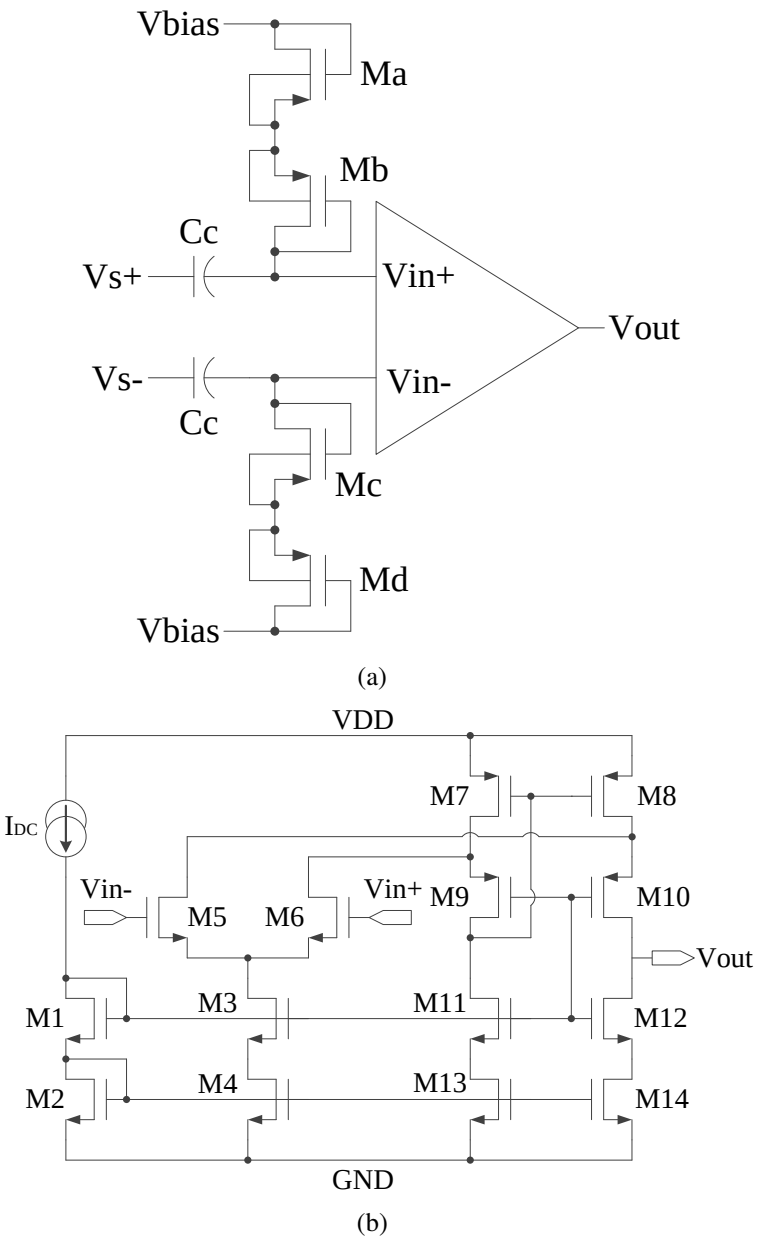


Figure 5: (a) Bioamplifier with a high-pass filter for DC suppression. (b) Schematic of the proposed bioamplifier.

biological neural signal is in the range of $50\mu V \sim 500\mu V$ and frequency ranges in $10 \sim 3$ kHz [**2**] [**10**]. Thus flicker noise is the dominant noise and the input stage that contributes the most flicker noise is the most noisy part in the circuit.

To design a low-noise amplifier, we can lower the total noise by reducing the noise contribution of the first stage, i.e. the noise contributed by $M_5 \sim M_8$. The thermal noise of the first stage can be expressed as

$$e_{ni,al}^2 = \frac{8kT\gamma}{g_{m5}} + \frac{8kT\gamma g_{m7,8}}{g_{m5}^2} \tag{3.4}$$

where k is the Boltzman constant and T is the absolute temperature. γ represents the drain noise coefficient. The flicker noise can be expressed as

$$e_{ni,flicker}^2 = \frac{2K_N}{C_{ox}(WL)_5 f} \tag{3.5}$$

where K_N represents the flicker noise coefficients, and C_{ox} is the gate oxide capacitance per unit area. Finally, the total input-referred noise can be represented as

$$v_{ni,rms} = \sqrt{\int_{BW} \left(e_{ni,thermal}^2 + e_{ni,flicker}^2\right) df} \tag{3.6}$$

By inserting (3.4) and (3.5) into (3.11), the equation (3.11) indicates that the total input-referred noise of the circuit can be reduced by enhancing the transconductances of M_5 and M_6. Large dimensions $\frac{348\ \mu m}{360\ nm}$ are used here to achieve high transconductance. Although the equation (3.4) also shows that by reducing the transconductance of $M_{7,8}$ pair can also reduce the noise, it can not be easily achieved because $M_{7,8}$ pair need to sustain a high current in the circuit which is the summation of current from input pair and output load. We applied a small aspect ratio, $\frac{14\ \mu m}{22\ \mu m}$, on $M_{7,8}$ pair for the purpose of a high gain in the first stage.

To evaluate the noise performance of a low-power bioamplifier, a commonly used performance metric is the NEF [**2**] that is expressed as

$$NEF = v_{ni,rms}\sqrt{\frac{2 \cdot I_{total}}{4\pi kT \cdot U_T \cdot BW}} \tag{3.7}$$

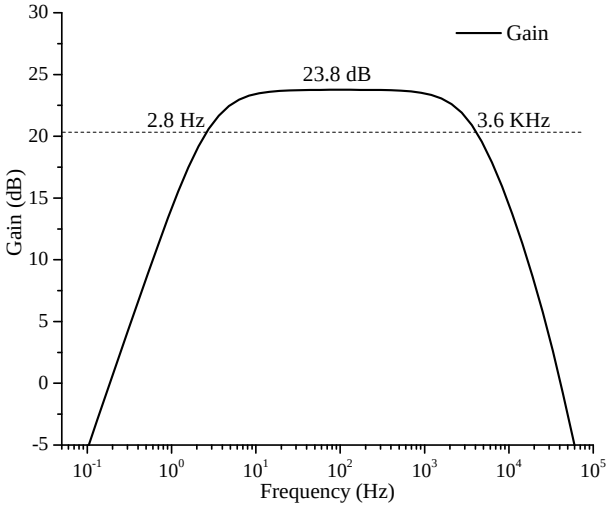


Figure 6: Gain and bandwidth profile.

where $v_{ni,rms}$ is the root mean square of input-referred noise, I_{total} is the total current, k is the Boltzman constant, T is the absolute temperature, U_T is the thermal voltage (26 mV@300K) and BW is the bandwidth.

Simulation Results

This design uses a standard 0.13-μm CMOS process and a 0.5 V supply. The proposed bioamplifier is designed and simulated with Cadence Virtuoso Spectre circuit simulator. The total power consumption including the high-pass filter is only 61.7 nW. In order to reduce flicker noise at the input stage, large dimensions $\frac{348\ \mu m}{360\ nm}$ are used on the input differential pair M_5 and M_6. The PMOS pair M_7 and M_8 sustain the largest drain current that prompts in a large drain noise. Therefore, to reduce the noise contribution, two PFETs have been used with a relatively small aspect ratio, $\frac{14\ \mu m}{22\ \mu m}$. Transistors $M_9 \sim M_{14}$ form the load current mirror which are biased by small drain current to achieve low transconductance.

By driving a load capacitor of 2 pF, the proposed bioamplifier produces a frequency response as shown in Fig. 6 As is seen from the plot, the bioamplifier achieves a gain of 23.8 dB and a -3 dB bandwidth of 3.6 kHz. The lower cutoff frequency, 2.8 Hz, is decided by the value of C_P and MOS-bipolar transistors, while the higher cutoff frequency, 3.6 kHz,

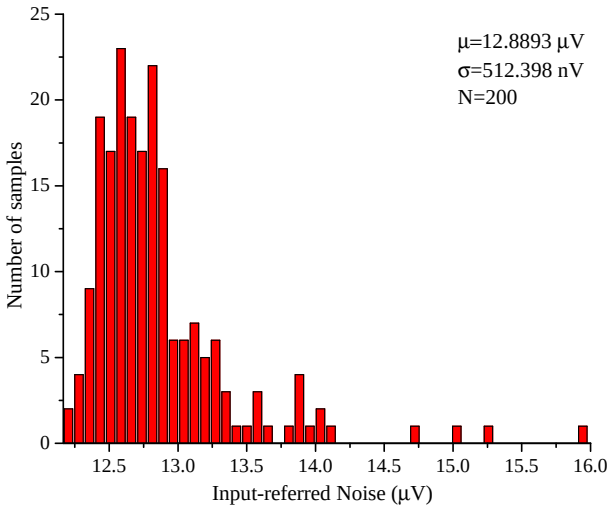


Figure 7: Monte Carlo Simulation. (a) Monte Carlo Simulation results of input-referred noise. (b) Monte Carlo Simulation results of THD when input V_{pp}=500 μV.

is determined by the output load capacitor and output resistance. In this design, C_P is 100 pf and are implemented with two Dual-MIMCAP capacitors.

The proposed bioamplifier achieves a 12.7 μV_{rms} input-referred noise in the noise simulation, that leads to a NEF of 3.1 under 61.7 nW power dissipation. Considering the process variation and mismatch of fabrication, Monte Carlo simulation is conducted to make a more practical assessment. Fig. 7(a) is the Monte Carlo simulation of input-referred noise with 200 samples. It produces a mean input-referred noise of 12.9 μV_{rms} with only 0.5 μV_{rms}

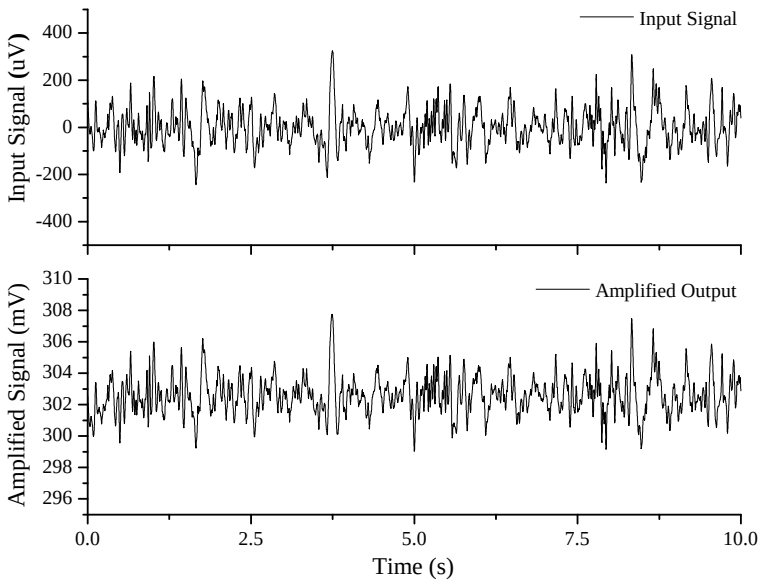


Figure 8: Input EEG signal and amplified output.

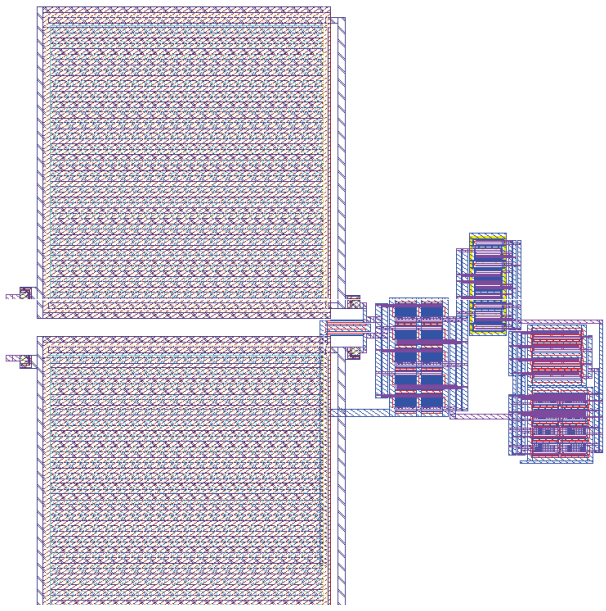


Figure 9: The layout of the proposed bioamplifier.

standard deviation. The relatively smaller standard deviation value indicates a robust noise performance of the proposed bioamplifier.

Linearity is another important parameter for an amplifier because it directly affects the dynamic range of amplifier and the fidelity of output signal. The transient simulation of

the proposed bioamplifier shows a 1% total harmonic distortion (THD) at the presence of 500 μV_{pp} input signal. Given a typical neural action potential has the amplitude in the range of $50 \sim 500\mu V$ [**27**], the linearity of the proposed bioamplifer is qualified for neural signal recordings. To verify the design for fabrication, another Monte Carlo simulation is done and the results are shown in Fig. 7(b). For a 500 μV_{pp} input signal, Monte Carlo simulation indicates a mean value of 1.2% THD and a standard deviation of ~ 0.33. The error between the transient simulation and the Monte Carlo simulation is due to the ultra-low-power design and the open-loop topology of the proposed bioamplifier.

A human EEG signal from MIT-BIH Database is applied to the proposed bioamplifier and the simulation results are shown in Fig. 8. The output indicates an identical dynamics but with a 23.8 dB amplification. The design has been submitted for fabrication and the layout is shown in Fig. 9. A comparison of the proposed bioamplifier with several existing works is shown in Table 1. The proposed circuit has a comparable noise and linearity performance with the previously published works, but consumes much less power, only 61.7 nW.

Table 1: Comparison of the Proposed Bioamplifier with the Previously Reported Works

	[**9**]	[**12**]	[**13**]	**This work**
Supply (V)	$\pm$0.9	1.5	1	0.5
Gain (dB)	28.9	37	40	23.8
f_L (Hz)	0.1-100	5	0.05	2.8
f_H (kHz)	11.2	7	10.5	3.6
$v_{ni,rms}(\mu V_{rms})$	14.5	5.5	2.2	12.7
NEF	1.95	2.58	2.9	3.1
1% THD (mV_{p-p})	-	0.40	1	0.5
Power (μW)	0.22	1.5	12	0.061
Technology (μm)	0.35	0.13	0.13	0.13
Year	2009	2011	2012	2012

Summary of Ultra-Low-Power Bioamplifier

In this study, we present the design of an ultra-low-power bioamplifier for biological signal recordings. Folded-cascode structure and subthreshold MOSFETs are used for low-power

low-noise amplification. The proposed amplifier has been designed and simulated in a standard 0.13-μm CMOS process. This amplifier has a gain of 23.8 dB with 3.6 kHz bandwidth and consumes only 61.7 nW from a 0.5 V power supply. The proposed amplifier has an input-referred noise of 12.7 μV_{rms} and a low NEF of 3.1.

A Low-Noise Gain-Tunable Amplifier

This study [**28**] presents a low-noise gain-tunable biopotential amplifier that is designed based on a folded-cascode structure. Sub-threshold and self-biasing techniques are employed to achieve a low-noise and low-power amplification. With a bias-current tuning block, the gain of the proposed biopotential amplifier can be precisely adjusted. Designed in a standard 0.13 μm CMOS process, the proposed amplifier provides a 5.9 kHz bandwidth and 30.1 dB gain with 732 nW power. The input-referred noise over the entire bandwidth is 4.3 μV_{rms}, equivalent to a noise-efficiency factor of 2.48.

Introduction of Low-Noise Gain-Tunable Amplifier

A biopotential amplifier [**2**][**7**] that amplifies neural signals at the front-end is one of the most important components of an implantable neural recording microsystem. Since neural signals typically range from 10 μV to 500 μV with a noise floor of 5 - 10 μV_{rms}, biopotential amplifiers must achieve both high gain and low-noise performance. Low-noise amplification is extremely important since it determines the sensitivity of the entire system as well as impacts the capacity of post-processing. Furthermore, due to the diversity of neural signals, different bandwidth ranges are expected to record different biosignals [**29**]. Finally, for all implantable circuit designs, power dissipation must be considered carefully since excessive power consumption will not only shorten the longevity of batteries but also cause the necrosis of tissues [**30**].

State-of-the-art biosignal amplifiers have achieved microvolt input-referred noise and sub-microwatt power dissipation. A neural amplifier [**9**] is reported to consume only 220

nW power with 14.5 μV_{rms} input-referred noise. The work presented in [**11**], reduces the input-referred noise to 3.5 μV_{rms} while consumes 7.92 μW power. Recently, a biopotential amplifier [**13**] which has a power dissipation of 12 μW achieves an input-referred noise of 2.2 μV_{rms}. With an improved power consumption of 800 nW, a neural recording amplifier [**31**] maintains the input-referred noise at 5.71 μV_{rms}.

In this work, we present a gain-tunable biopotential amplifier that achieves an input-referred noise of 4.3 μV_{rms} with 732 nW power consumption. The self-biasing arrangement consisted of weak inversion MOSFETs is demonstrated to achieve the low-noise and low-power amplification. The precisely tunable gain of the proposed amplifier can maximally utilize the resolution of an analog-to-digital converter (ADC) by adjusting the amplitude of the amplified signal to the suited range.

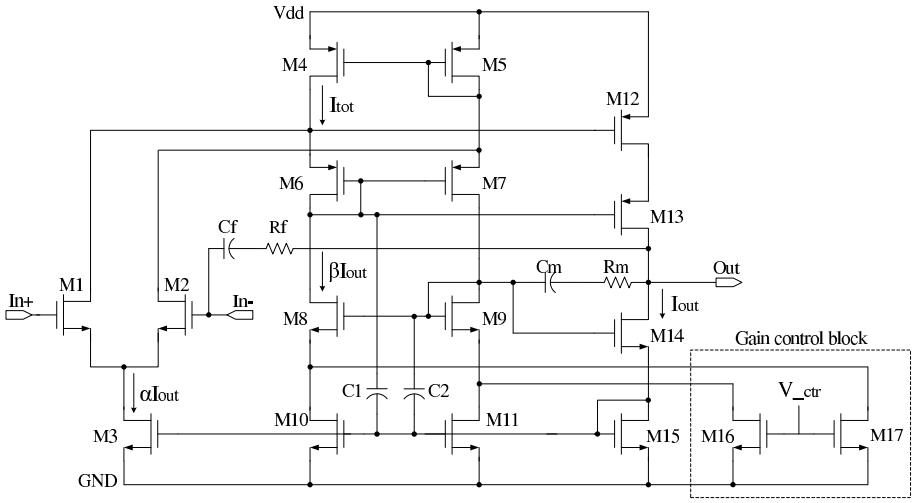


Figure 10: Schematic of the proposed biopotential amplifier.

Design of Proposed Biopotential Amplifier

Gain analysis.

Gain of stages: As shown in Fig. 10, the proposed amplifier consists of two stages - a folded-cascode stage (M_1-M_{11}) and an output stage (M_{12}-M_{15}). Transistors M_{16} and M_{17} are used to control the gain. Transistors M_{15}, M_3, and M_{10} creates the self-bias structure

for the DC bias of folded-cascode stage. If we represent the bias current of output stage as I_{out}, the drain current of M_3 and M_6 can be denoted as αI_{out} and βI_{out}, respectively where α and β are constants. Then, the drain current of M_4, I_{tot}, can be represented as:

$$I_{tot} = \frac{\alpha I_{out}}{2} + \beta I_{out} \tag{3.8}$$

By using EKV model [**32**] and ignoring the gain control block (M_{16} and M_{17}), we can obtain the gain of the folded-cascode stage:

$$A_1 = \frac{\left(nU_T + \frac{1}{\lambda_8 \lambda_{10} nU_T}\right)\left(\frac{1}{\lambda_8 \lambda_{10}(nU_T)^2+1}\right)}{2(\frac{\beta}{\alpha})\left[\lambda_4 (nU_T)^2 + nU_T + \frac{1}{\lambda_8 \lambda_{10}}\right] + (\lambda_1 + \lambda_4)\left[(nU_T)^2 + \frac{1}{\lambda_8 \lambda_{10}}\right]} \tag{3.9}$$

where λ and U_T represent the channel length modulation parameter and thermal voltage, respectively. The numeric in the subscript denotes the number of MOSFETs in Fig. 10. Similarly, the gain of output stage can be represented as:

$$A_2 = \frac{1}{\lambda_{15}(nU_T + \frac{1}{\lambda_{12}})} \tag{3.10}$$

The total gain, A_{OTA}, of the proposed amplifier is the multiplication of equations (3.9) and (3.10).

Gain control and bandwidth expansion: From equation (3.9), we may notice that α is proportional to A_{OTA}, while β is inversely proportional to A_{OTA}. In other words, the self-biasing arrangement of M_3 and M_{16} in Fig. 10 constitutes a positive feedback, while M_{10} and M_{16} create a negative feedback. Consequently, we can adjust the gain of the proposed amplifier by changing the value of β. A gain control block is added in the dashed line area of Fig. 10. When V_ctr rises, the drain current of M_{18} is increased. The current flow through $M_{6,7}$ and $M_{8,9}$ increases accordingly, which results in a bigger β value. As a result, the gain of the amplifier is decreased. In contrast, by lowering V_ctr, we can increase the gain accordingly. However, the change of V_ctr must keep all MOSFETs saturated in the weak inversion region. Both Miller feedback and external negative feedback are used on the proposed amplifier. Depicted in Fig. 10, C_m and R_m construct a miller feedback which

improves the stability by raising the phase margin. External negative feedback, C_f and R_f, expands the -3 dB bandwidth effectively, but at the expense of a few gain drop. C_1 and C_2 are added to improve the phase margin.

Noise Analysis. Since the input stage dominates the total noise contribution, we can estimate the noise performance of the entire amplifier by analyzing the input-referred noise of the input stage. To simplify the math, we represent the thermal noise and flicker noise from the pairs of $M_{1,2}$, $M_{4,5}$, $M_{6,7}$ as:

$$\overline{V_{n,in}^2} = 8kT\gamma\left(\frac{1}{g_{m1,2}} + \frac{g_{m4,5}}{g_{m1,2}^2} + \frac{g_{m6,7}}{g_{m1,2}^2}\right) + \frac{2K_N}{C_{ox}(WL)_{1,2}f} + \frac{2K_P}{C_{ox}(WL)_{4,5}f}\left(\frac{g_{m4,5}^2}{g_{m1,2}^2}\right) + \frac{2K_P}{C_{ox}(WL)_{6,7}f}\left(\frac{g_{m6,7}^2}{g_{m1,2}^2}\right) \tag{3.11}$$

where K_N and K_P are process-dependent constants; γ is MOSFET noise coefficient. The equation indicates that we can reduce both thermal noise and flicker noise by increasing the dimension of $M_{1,2}$. Although smaller $g_{m4,5}$ and $g_{m6,7}$ can also decrease the noise, lower transconductance will reduce the bandwidth of the amplifier. To strike a balance between noise and bandwidth, appropriate values of $g_{m4,5}$ and $g_{m6,7}$ are selected through simulation. Noise-efficiency factor (NEF) [**2**], which assesses noise performance along with power consumption and bandwidth, is also employed to make a complete evaluation on the proposed amplifier.

Simulation Results

The proposed biopotential amplifier is designed in a standard 0.13 μm CMOS process. As shown in Fig. 11(a), the frequency response of the proposed amplifier indicates a 30.1 dB gain and 5.9 kHz bandwidth, and 30° phase margin. Fig. 11(b) shows the variation of the gain corresponding to the change of V_ctr. By adjusting V_ctr from 30 mV to 105 mV, the gain of the amplifier can be tuned from 30.1 dB to 17.5 dB ($\sim$ -0.26 dB/mV). Fig. 12(a). presents the squared input noise over the -3 dB bandwidth of 3.4 Hz - 5.9

Table 2: Performance of the proposed amplifier and other state-of-art designs

	[**9**]^a	[**34**]^b	[**12**]^a	[**11**]^a	[**13**]^a	[**31**]^a	This work^b
$V_{ni,rms}$ (μV_{rms})	14.5	14.3	5.5	3.5	2.2	5.71	4.3
NEF	1.95	1.32	2.58	3.35	2.9	2.59	2.48
f_L (Hz)	0.1	0.024	5	10	0.05	0.2	3.4
f_H (kHz)	11.2	7.47	7	7.2	10.5	5.8	5.9
Gain (dB)	28.9	28.3	37	39.4	40	40	30.1
Supply (V)	$\pm$0.9	1.8	1.5	1.8	1	1	0.55
Power (μW)	0.22	0.077	1.5	7.9	12	0.8	0.732
1% THD (mV_{p-p})	-	-	0.4	5.7	1	-	3.6
Process (μm)	0.35	0.18	0.13	0.18	0.13	0.18	0.13

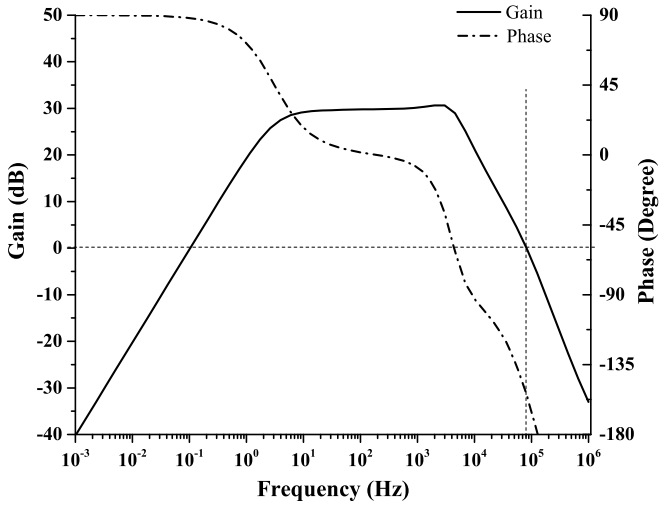
a: represents measurement results; *b*: represents simulation results.

kHz, which is equivalent to an input-referred noise of 4.3 μV$_{rms}$. A NEF of 2.48 can be calculated accordingly with a power consumption of 732 nW. The linearity of the proposed amplifier is examined with total harmonic distortion (THD). Fig. 12(b) shows the THD of amplified signals corresponding to different input peak-to-peak amplitudes. For a 1% THD, the peak-to-peak input signal is 3.6 mV. In order to verify the performance of the proposed amplifier in amplifying the real biopotential signals, a 47 years old female human electroencephalography (EEG) signal [**33**] is applied to the amplifier. As is seen in Fig. 13, the spike of input EEG signal has a magnitude of 129.8 μV, while the corresponding output spike achieves a magnitude of 4.4 mV. These values indicates an amplification of 33.9$\times$ or 30.6 dB, which is close to our ac simulation result of 30.1 dB gain. Table 2 summarizes the performance of this work and other state-of-art designs.

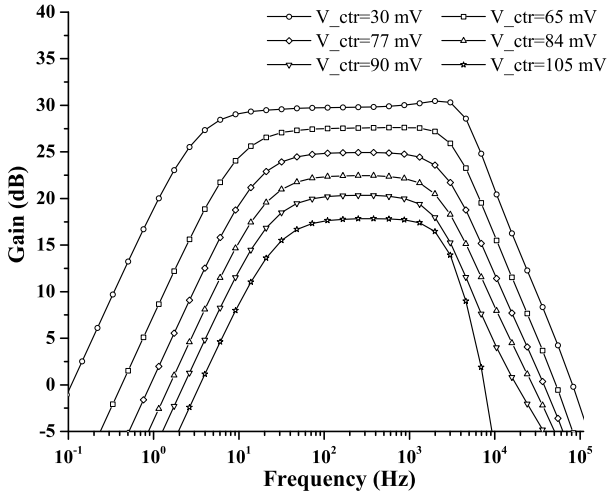
Summary of Low-Noise Gain-Tunable Amplifier

In this study, we have proposed an improved biopotential amplifier which achieves an input-referred noise of 4.3 μV_{rms}, corresponding to a NEF of 2.48. Owing to the subthreshold device and self-biasing scheme, the amplifier provides a 30.1 dB gain and 5.9 kHz bandwidth at the cost of only 732 nW power. The low-noise, low-power performance and tunable

gain make the proposed amplifier promising in the applications of large array neural signal recordings.

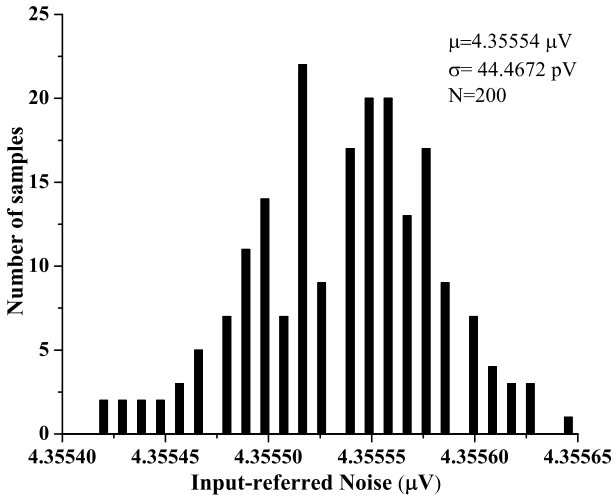


(a)

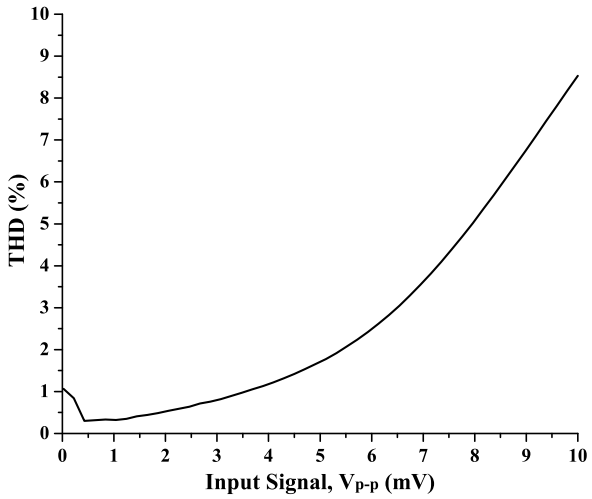


(b)

Figure 11: (a) Frequency response of the proposed amplifier. (b) The variation of gain controlled by different V_ctr.



(a)



(b)

Figure 12: (a) Monte Carlo simulation of input-referred noise. (b) The THD of output signals at different input peak-to-peak amplitudes.

Amplifier With Optimized Noise Efficient Factor

Implantable wireless neural recording microsystems have demonstrated their efficacies in neuroscience studies in the past decades. However, with the advances of neurobiology, higher sensitivity and higher precision neural recording microsystems are becoming the

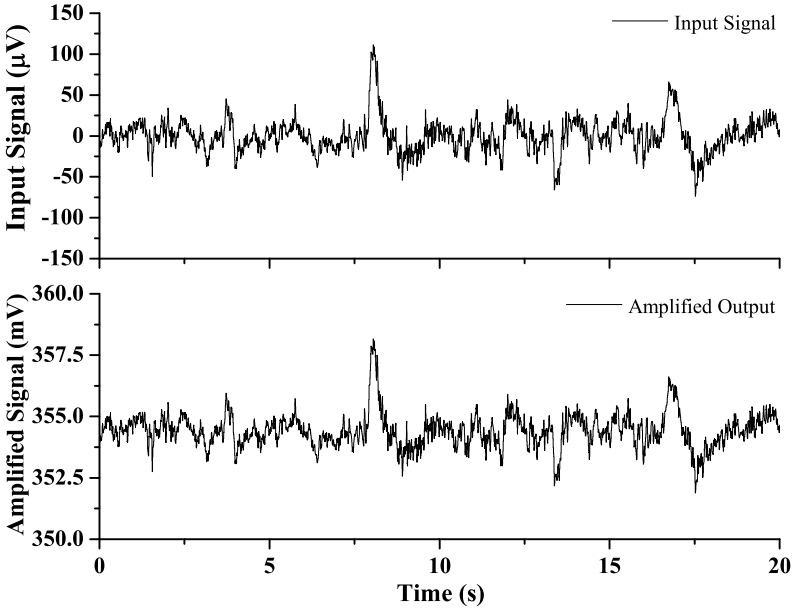


Figure 13: Performance verification of the proposed amplifier with EEG signals.

critical need. A biopotential amplifier is the first stage of a neural recording microsystem, the performance of which decides the signal-to-noise ratio and the power dissipation of each recording-channel. In this study, we present a low-noise biopotential amplifier with a noise efficiency factor (NEF) optimized closer to the theoretical limit of a folded cascode structure. A high transconductance input nMOSFET pair is designed to guarantee a low input-referred noise. A self-biased scheme comprising a weak positive feedback and a strong negative feedback is employed to further enhance the transconductance. By optimizing the noise performance while maintaining the NEF value close to the theoretical limit, a very low input-referred noise and a higher power-noise efficiency are achieved in our design. Using a standard 0.13-μm CMOS process, the proposed amplifier achieves an input-referred noise of 1.98 μV_{rms} at the expense of 7.5 μW power, corresponding to a NEF of 2.31. The gain of the proposed amplifier is 40.84 dB at a -3 dB bandwidth from 6.65 Hz to 9.38 kHz.

High-density neural recordings have the potential to help neuroscientists and clinicians revealing neural network mechanisms. New emerging implantable wireless neural recording microsystems[**35**] which can monitor a large amount of neural activities wirelessly have made the research of freely behaving animals possible. However, the design of an implantable wireless neural recording microsystem is challenging due to the properties of neural signals and the power constraint of implantable devices. A neural signal[**4**] is typically in the range of $10 \sim 500$ μV with a noise level of $5 \sim 10$ μV_{rms}, which demands a high-gain and low-noise amplification. In addition, as a heat flux of 80 mW/cm^2 can cause the necrosis of tissues[**2**], a low-power design is not only extending the lifetime of battery but also ensuring the safety of tissues.

A biopotential amplifier[**2**]-[**7**] which acts as the first amplification stage is one of the most important components in an implantable neural recording microsystem. The performance of a biopotential amplifier determines the complexity of the post signal processing. A well-designed low-power low-noise amplifier can improve the system sensitivity, dynamic range and power-efficiency. In the recent years, multiple high performance biopotential amplifiers[**4**]-[**13**] have been reported by pioneering researchers. Some of the research groups[**4**]·[**13**] have designed the biopotential amplifier with input-referred noise values in the range of $2 \sim 4$ μV_{rms}, but the power dissipation is usually larger than 10 μW. On the other side, some of the studies have developed amplifiers[**9**]·[**34**] with microwatt or sub-microwatt power dissipation, but the input-referred noise values are generally above 10 μV_{rms}. However, as the advances of neurobiology, high-sensitivity high-precision recordings have become a mandatory. It requires the design of amplifiers with $\sim$2 μV_{rms} input-referred noise while dissipating only a few microwatt power. To strike a balance on the noise performance and power dissipation, a numeric value called noise efficiency factor (NEF)[**2**] has been widely used by the researchers to evaluate the power-noise efficiency of their designs. A smaller NEF value indicates a higher power-noise efficiency which is preferred for a design.

In this work, we propose a low-noise biopotential amplifier with an NEF value close to the theoretical limit of the proposed circuit structure. The NEF theoretical limit of the proposed circuit topology is derived out first to guide the circuit design process. Based on this NEF value, we calculate the total current needed to achieve the highest power-noise efficiency. The very low input-referred noise is achieved by increasing the transconductance of the input nMOSFET pair. Three approaches are adopted here. Firstly, the nMOSFET pair are biased to operate at weak inversion saturation region for the high transconductance efficiency (g_m/I_D). Secondly, 1/3 of the total current is assigned to the nMOSFET pair. Thirdly, a self-biased structure comprising a weak positive feedback and a strong negative feedback is applied on the circuit to further enhance the transconductance.

The Proposed Low-noise Biopotential Amplifier

The overall schematic of the proposed biopotential amplifier is shown in the Fig. 14(a). It consists of a high-pass filter stage and an operational transconductance amplifier (OTA) based gain stage. The high-pass filter is created by the capacitors C_a, C_b and the equivalent resistors formed by the Miller effect of pseudoresistors $M_a \sim M_d$. The transistors $M_a \sim M_d$ are MOS-Bipolar pseudoresistors[**2**] which have the resistance in the range of 10$\sim$100 GΩ. Due to their large resistance values, the negative AC feedbacks created by the pseudoresistors have very small currents, which allows the gain of the proposed biopotential amplifier close to the open-loop gain of the OTA. In addition, the pseudoresistor connections also provide the DC biases for the gates of the transistors M_1 and M_2. By increasing the capacitances of C_a and C_b, a relatively small lower cut-off frequency can be obtained.

Fig. 14(b) shows the schematic of the proposed OTA circuit. The structure of the OTA circuit is based on the folded cascode structure. A 0.3 V bias voltage is applied on the gates of transistors M_7 and M_8. Unlike conventional folded cascode amplifiers, self-biased connections are applied on transistors $M_3 \sim M_6$ and $M_9 \sim M_{10}$. The reason to use the self-biased scheme is to form a positive feedback which can enhance the transconductance of the input nMOSFET pair. The positive feedback consists of transistors M_2, M_5, M_6,

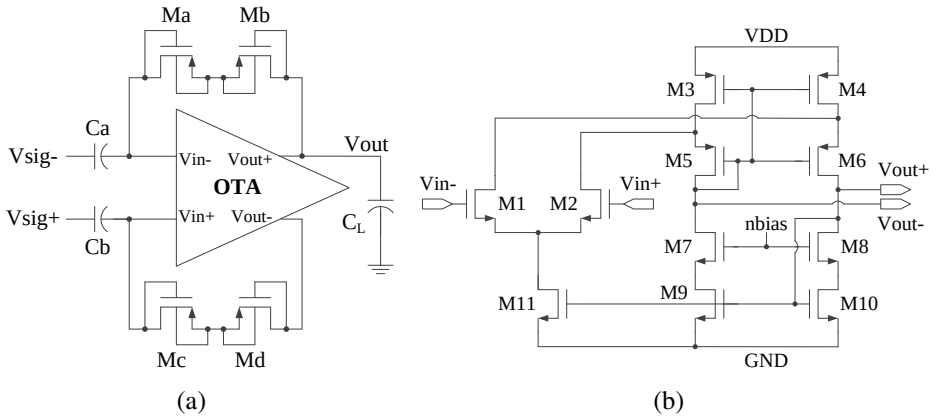


Figure 14: (a) The overall schematic of the proposed biopotential amplifier, (b) The schematic of the operational transconductance amplifier (OTA).

and M_{11}. The positive feedback mechanism can be explained as follows. When a neural signal is applied at the gate of transistor M_2, an amplified signal with 180° phase shift is generated at the drain of M_2. As transistor M_5 does not provide any phase shift, the same signal appears at the gate of M_6. By introducing another 180° phase shift due to gate-drain signal transition created by the transistor M_6, the signal appears at the gate of M_{11} has the same phase as the input signal. As a result, when a high voltage signal presents at the gate of transistor M_2, a high voltage also appears at the gate of transistor M_{11}, which increases the drain current of transistor M_{11} and eventually increases the bias current of the input nMOSFET pair. Since the drain current is proportional to the transconductance when a MOSFET operates at weak inversion saturation region, the increased bias current raises the transconductance of the input nMOSFET pair. Subsequently, an even larger high voltage is generated at the gate of transistor M_{11} and further boosts up the transconductance of the input nMOSFET pair. This positive feedback can increase the transconductance of the input nMOSFET pair to a certain degree, but it also lowers the signal linearity and circuit stability. Therefore, considering the linearity and stability requirements, a weak positive feedback is employed in the design to leverage the high gain performance. To guarantee the stability and linearity of the proposed biopotential amplifier, a strong negative feedback comprising transistors M_8 and M_{10} is created in the circuit. The operating principle of the

negative feedback can explained as follows. When the voltage at the gate of the transistor M_{11} rises, the drain current of the transistor M_{10} also increases resulting in a lower voltage at the drain of M_8. This reduces the voltage at the gate of transistor M_{10} and M_{11} and finally reaches a balanced output value.

We can obtain the gain of the proposed amplifier by deriving the gain of the OTA. Considering the perfect circuit symmetry, the transistor dimensions are identical for each pair, such as $M_1 - M_2$, $M_3 - M_4$, $M_5 - M_6$, etc. Thus, the gain of the proposed biopotential amplifier can be represented as

$$G = -g_{m1} \cdot [g_{m6} r_{o6} (r_{o4} || r_{o1}) || g_{m8} r_{o8} r_{o10}] \tag{3.12}$$

where g_m and r_o represent the transconductance and the output resistance of MOSFETs, respectively. From equation (3.12), we can notice that, in order to increase the gain, a large transconductance g_{m1} is desired. Thus, the transistors M_1 and M_2 are biased to operate at weak inversion saturation region for a high transconductance efficiency (g_m/I_D). As the transconductance of a MOSFET working in weak-inversion saturation region is proportional to its drain current, a large portion of the current from M_3 and M_4 is assigned to M_1 and M_2 to ensure the high transconductance.

Noise Performance Optimization

Since the biopotential amplifier is needed by each recording channel, its power dissipation must be kept at a very low level, typically a few micro-watt. For this reason, it is crucial to strike a balance on the power dissipation and the noise performance. Generally, the NEF is used to evaluate the power-noise efficiency of a design. In this work, we derive the NEF theoretical limit of a folded cascode amplifier first, and then we optimize the noise performance of the proposed biopotential amplifier following the NEF limit.

3.0.4. *NEF theoretical limit of a folded cascode amplifier*

The NEF value has been widely used by the low-noise biopotential amplifier designers in the previous works[**2**] - [**13**].

For the first step, we can model the total current of the circuit with some variables. As shown in Fig. 14(b), the total current dissipation, I_{total}, is the summation of currents flowing though transistors M_3 and M_4. Due to the symmetry, it is two times the drain current of transistor M_4. From Kirchhoff's current law, the drain current of transistor M_4 is equal to the summation of currents flowing through transistors M_1 and M_6. Here, we assume the drain current of transistor M_1 to be I_D and the drain current of transistor M_6 to be αI_D, where α represents the current ratio of transistor M_6 and M_1. Therefore, the I_{total} can be denoted as

$$I_{total} = 2I_D(1+\alpha) \tag{3.13}$$

For our second step, we will model the input-referred noise of the proposed amplifier, which consists of 1/f noise and thermal noise. The 1/f noise can be reduced by using large dimensions on the devices. Here we will only focus on the minimization of thermal noise. The major thermal noise of the circuit is from transistors $M_1 \sim M_4$, as they carry the largest currents in the circuit. However, as the noise of M_3 and M_4 will be divided by the amplifier gain, it can also be negligible. Therefore, for lower absolute theoretical limit, only the noise contribution from the thermal noise of the input nMOSFET pair is considered here and the corresponding input-referred noise can be depicted as

$$v_{ni,rms} = \sqrt{2 \cdot \frac{4kT\gamma}{g_{m1}} \cdot BW_{noise}} \tag{3.14}$$

where k is the Boltzmann constant, T is the absolute temperature, γ is the drain noise coefficient, and BW_{noise} is the noise bandwidth. For devices operating in weak inversion saturation region, the transconductances of transistors can be represented as

$$g_{m1} = \frac{I_D}{nU_T} \tag{3.15}$$

where n is the subthreshold slop factor and U_T is the thermal voltage (26 mV @ 300 K). If we consider the proposed biopotential amplifier as a one-pole system which has a dominant pole at the output, the noise bandwidth and -3 dB bandwidth have the relationship of

$$BW_{noise} = \frac{\pi}{2} \cdot BW \tag{3.16}$$

By taking equation (3.13) $\sim$ (3.16) into (**??**), we can arrive at

$$NEF = \sqrt{2n\gamma(1+\alpha)} \tag{3.17}$$

The value of noise coefficient γ is determined by the length of MOSFETs: 2/3 for long-channel devices and 2.5 for short-channel devices. The value of n is 1.4 in general. If we scale down the value of α close to zero, then the NEF theoretical limit of a folded cascode amplifier is in the range of 1.37 $\sim$ 2.65. Considering the flicker noise and the non-zero value of α, the practical value of NEF should be slightly larger than this approximation.

3.0.5. *Noise performance optimization under the NEF theoretical limit*

The input-referred noise is a standard benchmark used to characterize the noise performance of an amplifier. As the transistors $M_1 \sim M_4$ sustain the largest current in the circuit, the input-referred noise of the proposed amplifier can be represented by the noise from transistors $M_1 \sim M_4$ without the loss of generality. We will analyze the thermal noise and 1/f noise in the following paragraphs.

The input-referred thermal noise of the proposed biopotential amplifier can be represented as

$$\overline{v_{ni,th}^2} = 2 \cdot \frac{4kT\gamma}{g_{m1}} \left(1 + \frac{g_{m4}}{g_{m1}}\right) \tag{3.18}$$

where k is the Boltzmann constant, T is the absolute temperature, and γ is the drain noise coefficient. From equation (3.18), we can notice that, by increasing the transconductance g_{m1}, the thermal noise can be reduced. It is also possible to decrease the thermal noise by

lowering the transconductance g_{m4}. However, the latter is not possible in practice, since the transistor M_4 provides the current to maintain the operation bandwidth of the circuit.

The input-referred $1/f$ noise of the proposed biopotential amplifier can be expressed as

$$\overline{v_{ni,1/f}^2} = \frac{2K_N}{C_{ox}(WL)_1 f} + \frac{2K_P}{C_{ox}(WL)_4 f} \cdot \left(\frac{g_{m4}}{g_{m1}}\right)^2 \tag{3.19}$$

where K_N and K_P represent the 1/f noise coefficients of nMOSFET and pMOSFET, respectively. C_{ox} is the gate oxide capacitance per unit area. Again, a large transconductance g_{m1} can reduce the 1/f noise. In addition, equation (3.19) also indicates that, by applying large dimensions on the transistors M_1 - M_4, a lower 1/f noise can be achieved.

Based on the analysis mentioned above, a high transconductance on the input nMOSFET pair, transistors M_1 and M_2, is required to achieve the high-gain and low-noise performance. From equation (3.15), it is straightforward to increase the drain current as a method to achieve a high transconductance. However, the increasing of current may also raise the NEF value of the amplifier, which means a decreasing of the power-noise efficiency. Therefore, in order to achieve the low-noise performance while maintaining the NEF value close to the theoretical limit, we need to tune the circuits and compare the NEF value interactively.

Our strategy here is to decide the total current dissipation firstly. Based on the NEF theoretical limit obtained from previous section, the targeted input-referred noise (e.g. 2 μV_{rms}), and the required bandwidth (e.g. 9 kHz), we can calculate the smallest total current required to achieve the required performance. Secondly, we can select a relatively small value for the current ratio, α, and then scale the transistors to achieve the required ratio. Noise simulation is performed to find out the transistors contributing the most to the total noise. Then, the dimensions and aspect ratios of those transistors can be adjusted accordingly. A large amount of simulation tests are required here to strike a balance on the gain, bandwidth, and input-referred noise. The value of α may need to be reset if the targeted performance cannot be achieved. In the proposed biopotential amplifier, the value of α

Table 3: Transistor Aspect Ratios Used In the Proposed Amplifier.

Transistors	M_1,M_2	M_3,M_4	M_5,M_6	M_7,M_8	M_9,M_{10}	M_{11}
Aspect Ratios	$\frac{2\ mm}{0.64\ \mu m}$	$\frac{24\ \mu m}{16\ \mu m}$	$\frac{44\ \mu m}{0.8\ \mu m}$	$\frac{12\ \mu m}{18\ \mu m}$	$\frac{8\ \mu m}{20\ \mu m}$	$\frac{12\ \mu m}{10\ \mu m}$

selected is equal to 1/3, which means that 3/4 of the total current is assigned to the transistors M_1 and M_2. This setting creates a transconductance value, g_{m1}, up to 124.3 μs. In addition, the positive feedback formed by the self-biased connection of transistor M_{11} also enhances the transconductance g_{m1} by increasing the drain current of M_{11}. The other 1/4 of the total current is assigned to the transistors $M_5 \sim M_{10}$ to maintain the bandwidth and the load driving capability of the circuit. The transistor dimensions used in the proposed amplifier are presented in table 1.

Simulation Results

The proposed biopotential amplifier is designed using a standard 0.13-μm CMOS process and works with a 0.8 V supply voltage. The gain and phase responses of the proposed OTA are shown in Fig. 15(a). It shows that the proposed OTA achieves a gain of 41.22 dB and a higher cut-off frequency of 9.2 kHz by loading a capacitor of 1 pF. A phase angle of -91° is achieved at the 0 dB. Therefore, the phase margin of the OTA is 89°, which guarantees the stability of the proposed biopotential amplifier. Fig. 15(b) shows the frequency response of the proposed biopotential amplifier. It achieves a mid-band gain of 40.84 dB and a bandwidth of approximate 9 kHz by driving the same 1 pF load. The lower and higher cut-off frequency values are 6.65 Hz and 9.38 kHz, respectively. The small gain reduction comparing with the gain of the OTA is due to the bias connections formed by the transistors $M_a \sim M_d$.

The noise simulation of the circuits shows an input-referred noise of 1.98 μV_{rms} at the dissipation of 7.5 μW. As our design uses a 0.8 V supply voltage, a NEF value of 2.31 can be calculated with equation (**??**). To validate the stability of the circuits, 200 samples

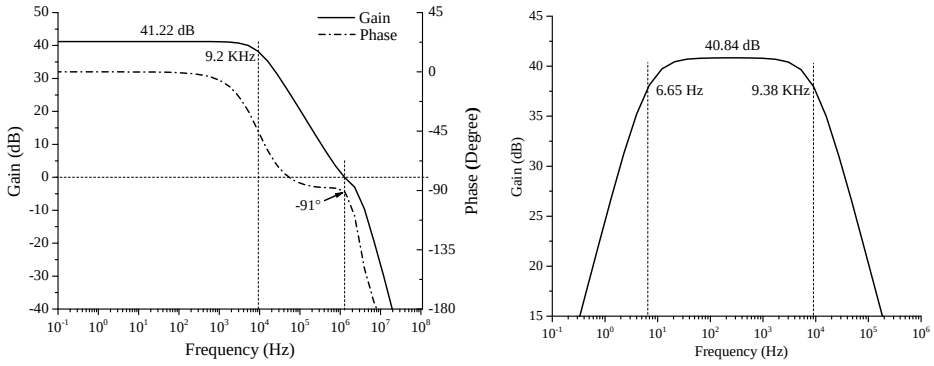


Figure 15: (a) The frequency response of the proposed OTA, (b) The frequency response of the proposed biopotential amplifier.

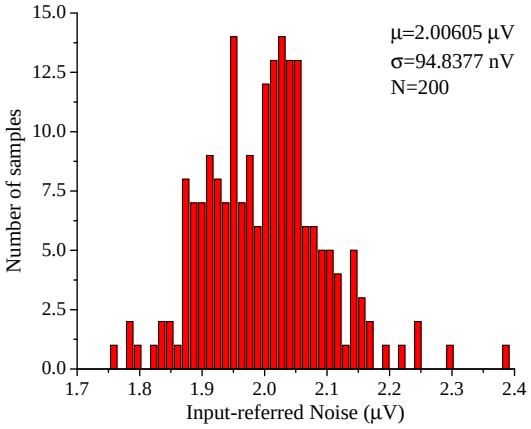


Figure 16: Monte Carlo simulation results of the input-referred noise .

Monte Carlo simulations have been done. As shown in Fig. 16, the Monte Carlo simulation exhibits a mean input-referred noise of 2 μV_{rms} with a standard deviation of 94.84 nV_{rms}.

Linearity is an important performance index for an amplifier since it decides the dynamic range of the circuits and the fidelity of the output signal. The maximum input peak-to-peak voltage to produce 1% total harmonic distortion (THD) is the value typically used to indicate the linearity of a amplifier. The transient simulation of the proposed amplifier exhibits a THD value of 0.3 mV_{pp}. The relatively smaller THD value is mainly due to the high gain and low supply voltage. However, given the amplitude of typical neural signals

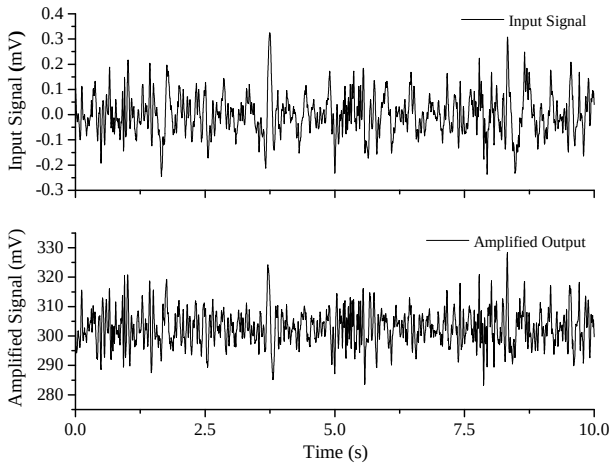


Figure 17: Input EEG signal and amplified output.

is in the range of $50 \sim 500\mu V$, the linearity of the proposed biopotential amplifier is still applicable for the biosignal amplification.

Finally, to estimate the performance of the proposed biopotential amplifier in amplifying real neural signals, a human electroencephalography (EEG) signal from MIT-BIH Database is applied to the amplifier. The transient simulation results are shown in Fig. 17. The amplified output indicates a gain of 110, or 40.84 dB. A comparison of the proposed amplifier with several other previously reported works is shown in Table 2. The proposed biopotential amplifier achieves the lowest input-referred noise (1.98 μV_{rms}) and NEF value (2.31), while maintains comparable performance in terms of power dissipation, gain, bandwidth, and THD values.

Summary of Amplifier With Optimized Noise Efficient Factor

This study presents a low-noise biopotential amplifier with an NEF value close to the theoretical limit of the folded cascode structure. In order to achieve the low-noise amplification at the highest power-noise efficiency, the total current dissipation required to maintain the NEF close to the theoretical limit is calculated firstly. Then, 3/4 of the total current is assigned to the input nMOSFET pair for a high transconductance. To further enhance the transconductance, a self-biased structure comprising a weak positive feedback and a strong

Table 4: A comparison of reported biopotential amplifiers.

	12^a	13^a	20^a	21^a	22^b	This work^b
$V_{ni,rms}$ (μV_{rms})	3.5	5.5	5.71	2.2	4.3	1.98
NEF	3.35	2.58	2.59	2.9	2.48	2.31
f_L (Hz)	10	5	0.2	0.05	3.4	6.65
f_H (kHz)	7.2	7	5.8	10.5	5.9	9.38
Gain (dB)	39.4	37	40	40	30.1	40.84
Supply (V)	1.8	1.5	1	1	0.55	0.8
Power (μW)	7.9	1.5	0.8	12	0.732	7.5
1% THD (mV_{pp})	5.7	0.4	-	1	3.6	0.3
Technology (μm)	0.18	0.13	0.18	0.13	0.13	0.13
Year	2011	2011	2012	2012	2013	2013

negative feedback is employed. With a standard 0.13-μm CMOS process, the proposed amplifier achieves an input-referred noise of 1.98 μV_{rms} at the expense of 7.5 μW power, corresponding to a NEF of 2.31. The mid-band gain of the proposed biopotential amplifier is 40.84 dB with a -3 dB bandwidth of $\sim$9 kHz.

4. NEURAL SPIKE DETECTOR

Low-Power High-Sensitivity Spike Detectors

A spike detector has become a necessity of a contemporary multichannel neural recording microsystem for data-compression. This work [**44**] [**45**] proposes two spike detection algorithms, frequency-enhanced nonlinear energy operator (fNEO) and energy-of-derivative (ED), to solve the sensitivity degradation suffered by the conventional nonlinear energy operator (NEO) at the presence of large-amplitude baseline interferences. The efficiency of NEO, fNEO and ED algorithms are evaluated with Simulink programs firstly and then implemented into three low-power spike detectors with a standard 0.13-μm CMOS process. To achieve a low-power design, subthreshold CMOS analog multipliers, derivatives and adders are developed to work with a low supply voltage, 0.5 V. The power dissipation of the proposed fNEO spike detector and ED spike detector are only 258.7 nW and 129.4 nW, respectively. The quantitative investigation shown in the study indicates that both fNEO and ED spike detectors achieves superior performance than the conventional NEO spike detector. Considering its lowest power dissipation, the ED spike detector is selected for our application. Further statistical evaluations based on the true positive and false positive detection rate proves that the ED spike detectors achieves higher detection rate than that of the conventional NEO spike detector but dissipates 48% less power.

Introduction of Spike Detectors

Implantable wireless neural recording microsystems have been extensively used in the studies of neurobiology and brain-machine interface. State-of-the-art implantable wireless neural recording microsystems [**46**]-[**48**] have already achieved the capability of real-time monitoring of neural signals over 100 channels. However, the increasing of recording channels gives rise to a larger data volume which demands higher data rate and higher bandwidth for

data transmission. For example, a 100-channel microsystem, with a sampling frequency of 24 kHz per channel and 10 bits per sample, requires a transmission bandwidth of 24 Mbps [**49**]. Since the existing telemetry link for biomedical applications is typically 1-2 Mbps, it is a big challenge for the transmitter design considering the low-power requirement of the implantable microsystems.

A carefully designed spike detector can effectively reduce the power dissipation of a microsystem by minimizing the transmission data. Given the low occurrence rate of neural action potentials (APs), about 10 to 120 occurrences per second, it is promising to achieve a large data compression by removing the redundant data at the intervals of spikes. Although a spike detector itself may dissipate some power, comparing with the large power reduction (up to 5 times) brought by the data compression [**49**], the introduction of a low-power spike detector is still an effective power reduction strategy.

A spike detection algorithm is the core of a spike detector. A variety of mathematical tools have been employed for the design of spike detection methods, such as thresholding [**50**]-[**51**], spike derivatives [**52**][**53**], and energy operators [**54**][**55**]. Because of its low computation complexity, robust and unsupervised features, the nonlinear energy operator (NEO) [**55**]-[**59**] has become the mostly used approach. The low-power NEO spike detectors have been extensively reported in the past years. Based on the sub-threshold design, a NEO spike detector [**56**] achieves a power dissipation of 2.7 μW. Another study [**57**] combining the NEO spike detector and the spike feature extractor together dissipates only 1 μW power. A NEO spike detector [**58**] which improves the detected waveform integrity has achieved a power dissipation as low as 780 nW. However, these studies only target on the neural spike signals with a constant signal baseline and fail to address the impact of large-amplitude baseline interferences. These interferences which consist of the local field potentials (LFPs) and the APs from neighbouring neurons are inevitably superimposed on the neural spike signals during the recording. Since LFPs contain important information for the clinical applications, such as epileptic seizure [**60**], it is desired to keep them in the recorded signals and should not be filtered out. However, the LFPs have the amplitude as

high as 1 mV and frequency up to 200 Hz [**21**] which may create a challenge for the spike detection considering that the amplitude of neural spike signals is typically in the range of 50-500 μV.

Our previous study [**44**] has shown the sensitivity degradation of conventional NEO spike detectors at the presence of LFPs. In this work, we extended our previous work by incorporating a comprehensive evaluation on the detection accuracy of the proposed spike detectors. In second part, the characteristics of three mostly used spike detection algorithms are introduced briefly. The third part elaborates the principles of the proposed spike detection algorithms, namely frequency-enhanced NEO (fNEO) and energy-of-derivative (ED), and compares them with NEO method. In the fourth part, the NEO, fNEO, and ED algorithms are implemented into three low-power full-analog spike detectors and the performance of the proposed algorithms are verified with the implemented spike detectors. A large amount of statistical evaluations have been made in the fifth part to demonstrate the detection robustness of the proposed ED spike detector at different signal-to-noise ratio (SNR). Finally, we conclude this work in the last.

Background on Detection Algorithms

Direct thresholding, time-derivative and NEO are the three major approaches used in CMOS integrated spike detectors. In this section, these schemes are explained briefly.

Direct thresholding method [**50**]-[**51**] discriminates APs from background signal by directly comparing input signal with a pre-setting or system self-acquired threshold. It has the least computation and lowest power consumption. However, the accuracy of thresholding method relies highly on the selection of threshold and decreases rapidly with the drop of SNR. New methods such as absolute thresholding and adaptive thresholding [**15**] have improved the detection rate, but the accuracy still decreases for low SNR input signal.

Time-derivative method [**52**][**53**] computes the derivative of input with respect to time and then use thresholding to discriminate spikes from derivative result. This method enhances the sensitivity of detectors by emphasizing the high-frequency spectrum which

manifests the waveform difference contributed by neurons and background noise. However, in many applications, the derivative results are still very small comparing with large background noise, and therefore, the detection rate of time-derivative method still needs to improve.

NEO is proved by previous studies [**55**] as an optimal choice for spike detections when input signal has low SNR. The mathematical model of NEO can be represented as

$$\psi_{NEO}(f(t)) = \left(\frac{df(t)}{dt}\right)^2 - f(t)\left(\frac{d^2f(t)}{dt^2}\right) \tag{4.1}$$

If the input has only one frequency, i.e. $f(t) = Asin(\omega t)$, where A and ω denote the amplitude and frequency, respectively, the output of NEO is a constant value, $A^2\omega^2$. The spike signals which hold relatively high frequency and large amplitude have the strongest output. However, in practical neural signal recordings, the amplitude of spikes can be much smaller than that of low-frequency interference, which trades off its weight on frequency.

Proposed Spike Detection Algorithms

To overcome the performance degradation of NEO method, we propose two approaches, fNEO and ED, by enhancing the weight of frequency in the algorithm.

The mathematical model of fNEO can be represented as

$$\psi_{fNEO}(f(t)) = \left(\frac{d^2f(t)}{dt^2}\right)^2 - \frac{df(t)}{dt}\left(\frac{d^3f(t)}{dt^3}\right) \tag{4.2}$$

For the same single-frequency signal, $f(t) = Asin(\omega t)$, the output of fNEO is $A^2\omega^4$ which indicates an enhanced weight on the frequency of input signal. Equation 4.2 also indicates that fNEO is actually an approach that applies NEO method on the derivative of the input signal.

As the interference is a relatively low-frequency signal, it degrades the performance of NEO through the second term of Equation 4.1. Therefore, we can remove the second term

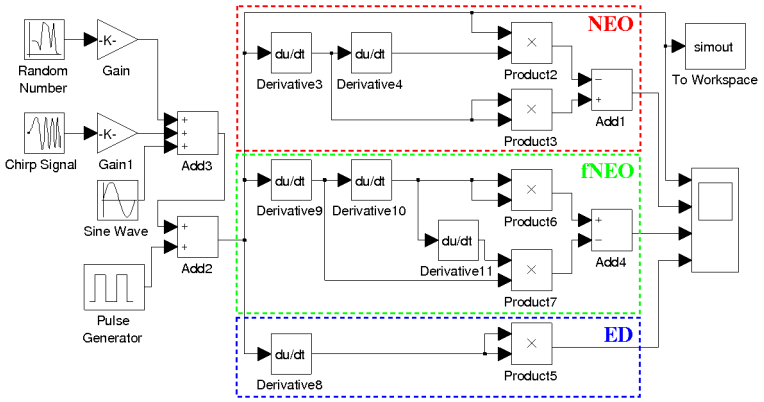


Figure 18: Simulink models of NEO, fNEO and ED.

and arrive at the ED method which can be represented as

$$\psi_{ED}(f(t)) = \left(\frac{df(t)}{dt}\right)^2 \tag{4.3}$$

The output of the single-frequency signal, $f(t) = Asin(\omega t)$, is $A^2\omega^2/2 + A^2\omega^2 cos(2\omega t)/2$, where the second term can be removed as 2ω is out of the circuit operation band.

Three algorithms, NEO, fNEO and ED, are investigated in MATLAB Simulink as shown in Fig. 18 with synthesized neural spike signals. The synthesized spikes have 1 ms width and 100 Hz firing rate (FR) which is aimed to imitate the real neural APs generated by the voltage-gated sodium-channel [**21**]. Gaussian white noise is added on the signal. An extra interference varying from 0.1 $\sim$ 300 Hz is added to imitate the baseline interference. Simulation results of NEO, fNEO and ED algorithms are shown in Fig. 19. The detected spikes with conventional NEO method have a large variation on their amplitudes. A few spikes, such as the spike at 0.02 s, are even smaller than the noise signal, which may result in spike missing during the detection. In contrast, the proposed fNEO and ED hold a higher consistency on the amplitude of detected spikes. Besides, the results also show that the fNEO and the ED have higher noise suppression features than conventional NEO. To make a quantitative and objective evaluation, standard deviation (STD) and peak-to-clutter ratio (PCR) are employed to analyse the detected signal. For a fair comparison of STD analysis, all of the output signals are normalized first with respect to the corresponding

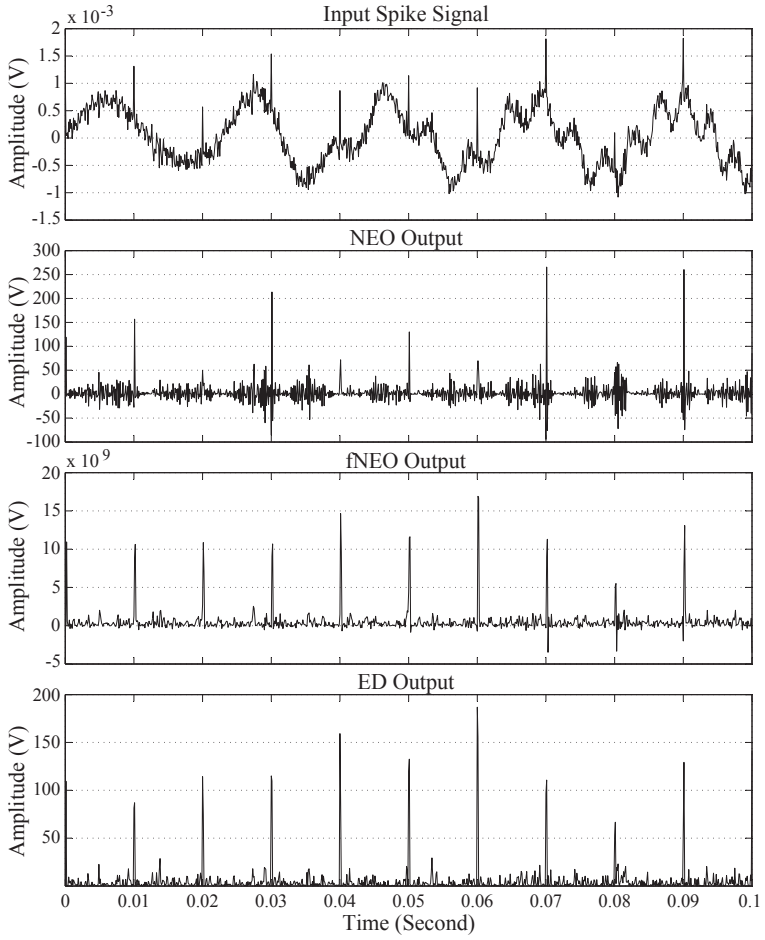


Figure 19: Simulink algorithm simulation results of three methods. Input signal: a combination of neural spike signals, Gaussian white noise, and baseline interferences

absolute maximum values. Then, the STD value, σ, of the normalized output is calculated as

$$\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - \mu)^2}, \text{where } \mu = \frac{1}{N}\sum_{i=1}^{N} x_i \tag{4.4}$$

The value of σ reflects the consistency of detected peak values. On the other hand, PCR is an effective number which decides the detection accuracy of thresholding stage. The PCR is defined as

$$PCR = \frac{|\, V_{spike} \,|_{min}}{|\, V_{noise} \,|_{max}} \tag{4.5}$$

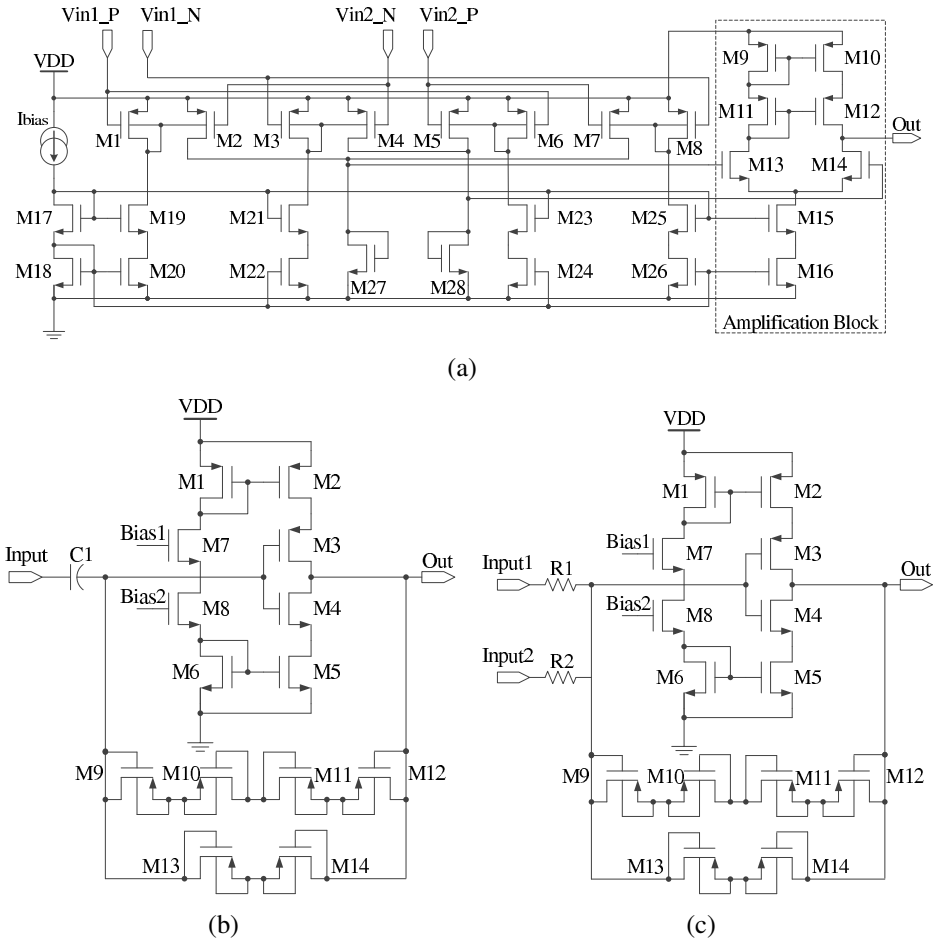


Figure 20: The major building blocks of NEO spike detectors: (a) Multiplier, (b) Derivative, and (c) Adder.

where $|V_{spike}|_{min}$ and $|V_{noise}|_{max}$ are the amplitudes of the minimum detected spike and the maximum noise level, respectively. Larger PCR value means larger difference between the signal and the noise which can reduce the false alarm of the detection. Table 1 presents the STD and PCR values of algorithm simulation. It shows that conventional NEO has a 1.7 times higher STD than those of fNEO and ED, while its PCR is about 2.7 times smaller than those of fNEO and ED.

Table 5: Sensitivity comparison of three spike detectors.

	Parameters	NEO	fNEO	ED
Algorithm	σ	0.307	0.176	0.182
	PCR	0.792	2.173	2.046
Circuit	σ	0.0965	0.0592	0.0669
	PCR	0.963	1.134	1.128

The Low-power Analog Implementations

Previous spike detectors are typically implemented with operational transconductance amplifier (op-amp) [**58**] or translinear circuits [**61**][**56**]. Here, we implement the proposed algorithms with inverter based circuits for the purpose of power reduction. The designs use a 0.5 V power supply and all the transistors work in weak-inversion. The primary building blocks of the proposed spike detectors are multipliers, derivatives, and adders.

A weak-inversion analog four-quadrant multiplier is designed based on the body-drain-connected structure [**62**], shown in Fig. 20(a). V_{in1_P}, V_{in1_N}, V_{in2_P} and V_{in2_N} are the four ports of two differential pairs. An amplification block shown in the dashed line of Fig. 20(a), is added to compensate the loss of signal strength and also to improve the SNR. Transistors $M_{17} \sim M_{26}$ create the bias circuits for the multiplier, while M_{15} and M_{16} serve as the current source for the amplification block. The output of the multiplier can be expressed as

$$V_{out} = \left(\frac{4 I_{bias} V_{in1} V_{in2}}{(nU_T)^2 g_{m_{27,28}}} \right) \cdot g_{m_{13,14}} (r_{o_{14}} || g_{m_{12}} r_{o_{12}} r_{o_{10}}) \tag{4.6}$$

The power dissipation of the multiplier block is 89.6 nW.

Low-power derivative circuits can be achieved by replacing op-amps of classic derivative circuits with a high-gain inverter [**63**]. However, the bias circuits must be carefully designed to guarantee system reliability. Fig. 20(b) is a digital inverter based derivative circuit where M_3 and M_4 form the digital inverter structure. M_7 and M_8 serve as a current source which is biased by *Bias*1 and *Bias*2. By carefully tuning the dimensions of the transistors $M_1 \sim M_6$, the sinking and sourcing currents of the inverter can be controlled at a smaller value and hence restrict the power dissipation of the circuit. $M_9 \sim M_{14}$ are

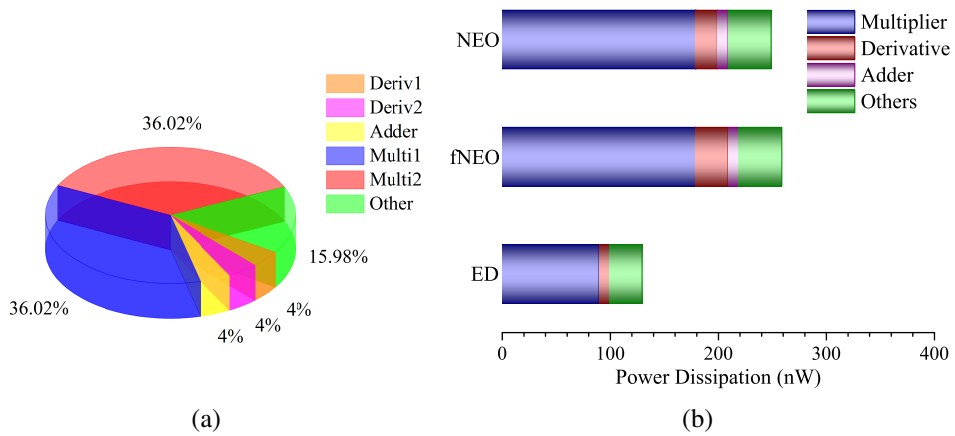


Figure 21: (a) Power budget of a conventional NEO spike detector, (b) Power dissipation of NEO, fNEO, and ED spike detectors.

Tobi-elements [**63**] which have very high impedances. The input and output of the digital inverter are biased at $V_{DD}/2$ by the high impedance path formed by $M_9 \sim M_{12}$. High impedances of M_{13} and M_{14} allow the use of smaller capacitor to achieve a relatively high output voltage. The total power dissipation of the proposed derivative circuit is 9.9 nW. By replacing the capacitor with two polysilicon resistors, R_1 and R_2, a two-input adder circuit can be built as shown in Fig. 20(c). The power dissipation of the proposed adder is 9.9 nW.

To implement a conventional NEO spike detector, two derivative circuits, two multipliers and one adder are needed. The power budget of NEO spike detector is shown in Fig. 21(a). We can see that multipliers are the most power hungry parts, while derivative circuits cost only a small portion of power. Therefore, a fNEO spike detector that has one additional derivative block than a NEO spike detector can achieve higher sensitivity at the expense of only $\sim 4\%$ higher power. By reducing one multiplier block, the ED spike detector offers 48% less power than NEO with comparable sensitivity. Fig. 21(b) shows a comparison on the power dissipations of the three spike detectors.

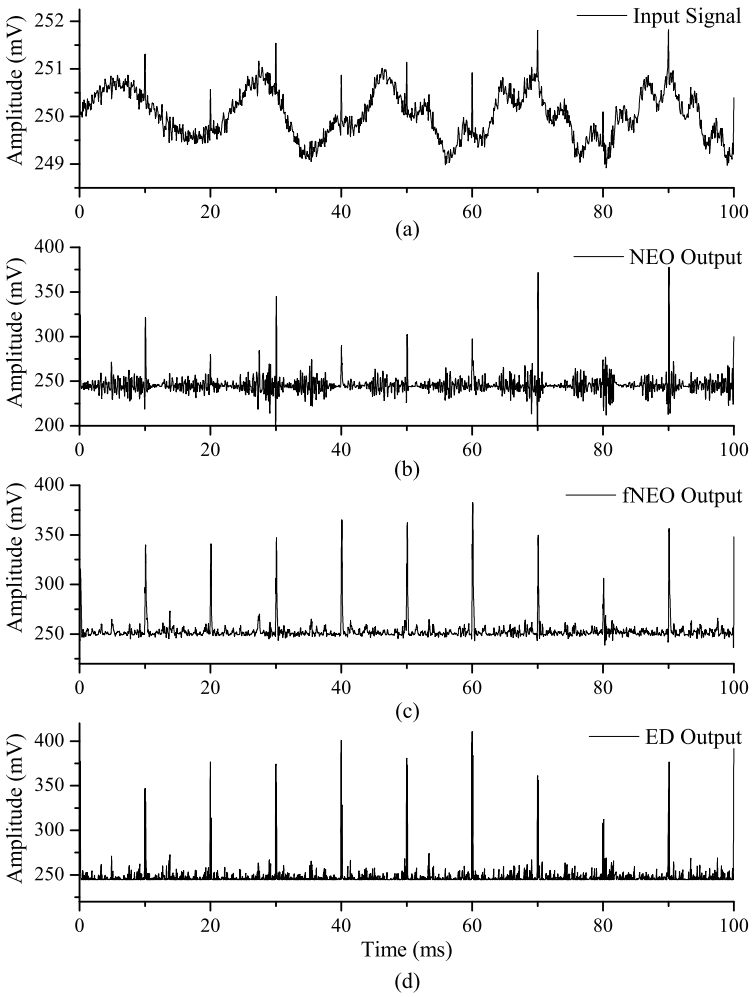


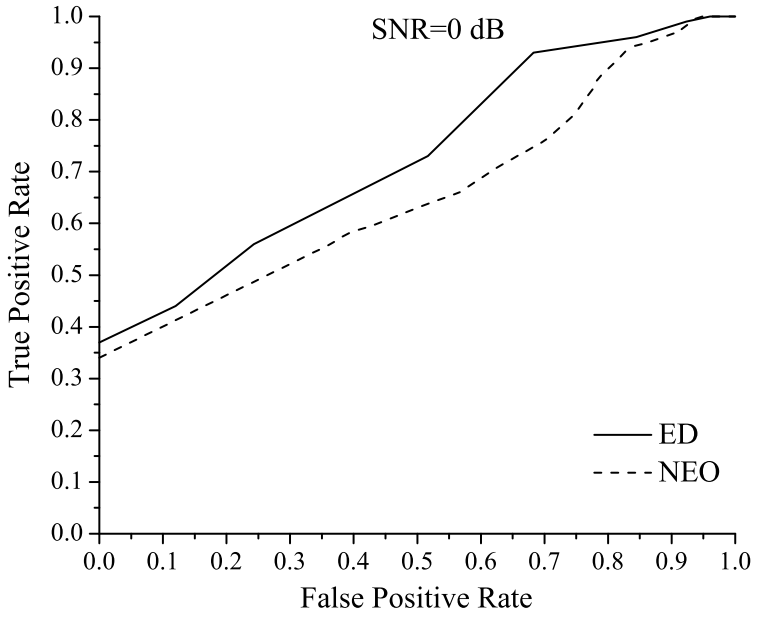
Figure 22: Cadence circuit simulation results of three spike detectors. (a) Input signal: a combination of neural spike signals, Gaussian white noise, and baseline interferences, (b) NEO spike detector output, (c) fNEO spike detector output, (c) ED spike detector output.

Simulation Results and Statistical Analysis

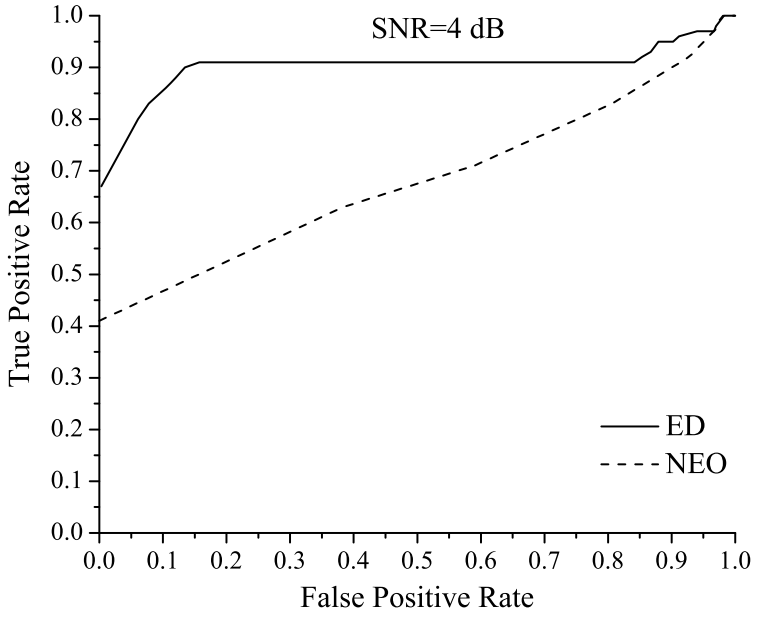
The identical synthesized input signal as used in Fig. 19 is applied to the implemented spike detectors and the corresponding outputs are shown in Fig. 22. Comparable with the results shown in Fig. 19, the circuit simulation results of fNEO and ED spike detectors also exhibit superior performances than that of NEO spike detector in terms of output spike consistency and noise floor. Table 1 summarizes the σ and PCR values calculated from the algorithm and circuit simulation results. The circuit simulation results indicate that fNEO and ED spike detectors achieve 38.65% and 30.67% smaller σ, respectively, than

that of NEO spike detector, while the PCR values of fNEO and ED spike detector outputs are 17.76% and 17.13% larger, respectively, than that of NEO spike detector. It has been demonstrated that fNEO and ED spike detectors hold higher consistency on the output spike signals and produce larger signal differences between the neural spikes and the background noise, which benefits the discrimination of neural spike signals from background. The relatively small improvement on PCR values is a trade-off of the low-power design. Since we use a low supply voltage (0.5 V) to achieve the low-power performance, the dynamic range of the circuits is limited, which affects the improvements of PCR values. Besides, the thermal noise and flicker noise from the spike detector circuits can also be a factor to affect the PCR values. In general, since the ED spike detector holds comparable performance as fNEO but dissipates about 50% less power, we select ED spike detector for our application.

To further evaluate the detection robustness of the proposed ED spike detector, the synthesized neural spike signals with SNR values varying from -5 dB to 10 dB are applied to the spike detectors. Each group of the synthesized spike signals contains 100 pulses where each pulse has 1 ms duration and fires at 100 Hz. These values are selected to imitate the APs from brain cells. The sampling frequency of the synthesized signal is 50 kHz. Gaussian white noise is added on the signal to produce the noise degraded spike signals with SNR values ranging from -5 dB to 10 dB. An interference signal with 1 mV amplitude and up to 300 Hz frequency is superimposed on the noise degraded spike signals to mimic the impact of LFPs. In order to obtain a large number of test trials demanded by the statistical evaluation, a Cadence OCEAN Script is used to control the co-simulation between MATLAB and Cadence Virtuoso Spectre circuit simulator. While MATLAB codes are responsible for the signal generation, spike counting, statistical calculation, data plotting and saving, the Cadence OCEAN Script controls the circuit simulation environment and the output of results. Based on the results from the co-simulation, the receiver operating characteristic (ROC) curves are drawn for both the ED spike detector and the NEO spike detector, as shown in Fig. 23. The ROC curve of a spike detector depicts the true positive rate (TPR)



(a)



(b)

Figure 23: (a) The receiver operating characteristic (ROC) curves of the proposed ED spike detector and NEO spike detector at SNR = 0 dB, (b) The ROC curves of the proposed ED spike detector and NEO spike detector at SNR = 4 dB.

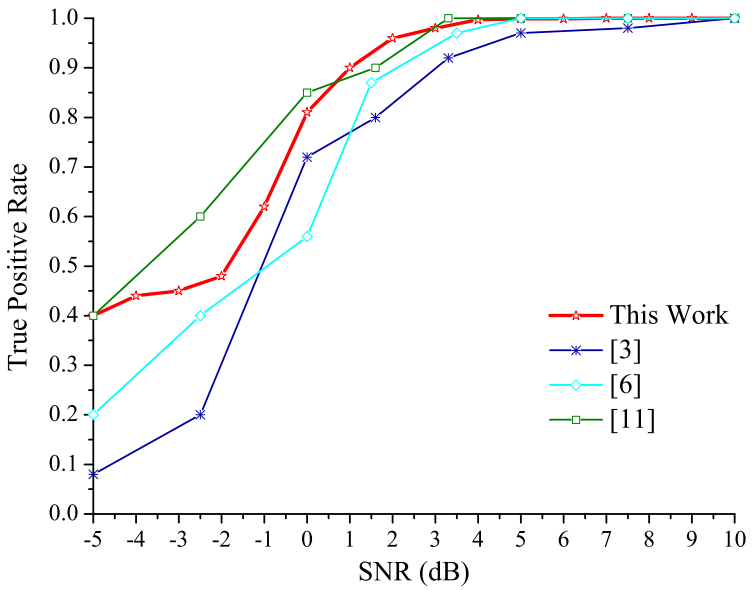
against the false positive rate (FPR) at different threshold values. Here, the TPR is defined as

$$TPR = \frac{the\ number\ of\ spikes\ correctly\ detected}{the\ number\ of\ spikes\ inserted} \tag{4.7}$$

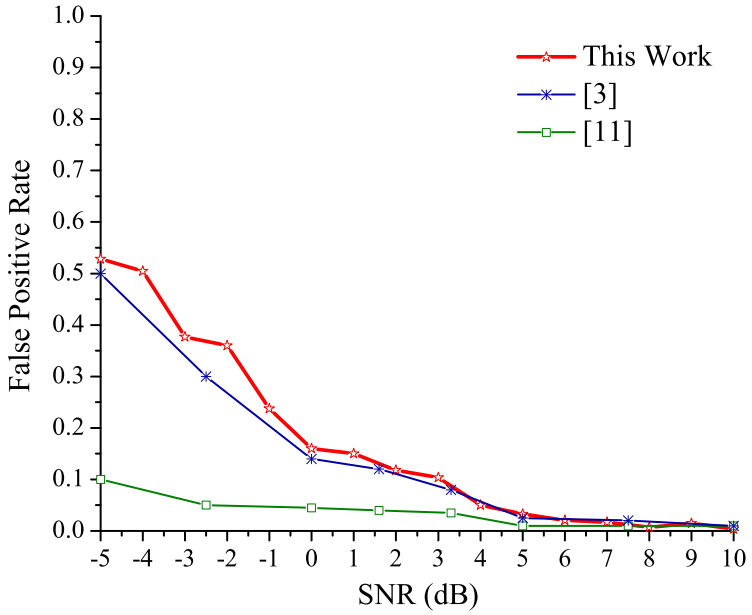
The FPR is defined as

$$FPR = \frac{the\ number\ of\ false\ detections}{the\ total\ number\ of\ detections} \tag{4.8}$$

In terms of spike detections, TPR is equivalent to the detection rate, while FPR is equivalent to the false alarm rate. Thus, for a ROC curve, the closer to the top-left of the ROC plot the better is the performance the spike detector. From Fig. 23, we can see that the ED spike detector achieves higher detection rate than that of NEO spike detector at both SNR=0 dB and SNR=4 dB. This improvement becomes larger when SNR is 4 dB. It is supported by other simulation results that the improvement of detection rate brought by the ED spike detector becomes larger when the SNR value increases and *vice versa*. In order to make a comparison with the previously reported spike detectors, the noise degraded spike signals without the baseline interference is applied to the ED spike detector. The TPR and FPR values of the proposed ED spike detector at different SNR values are drawn in Fig. 24. In Fig. 24, the studies [**15**][**55**] are computational simulation results which are similar to our algorithm based simulation results shown in the third part, while the study [**48**] is chip measurement result. From Fig. 24(a), we can see that the proposed ED spike detector has a slow increase on the value of TPR when the SNR value is smaller than -2.3 dB. However, after that, it increases rapidly and finally outperforms other spike detectors when the SNR value is larger than 1 dB. It indicates that, for a recorded neural spike signals with SNR $>$1 dB, the ED spike detector can achieve the highest detection rate. Since not many previous studies include a complete statistical study, Fig. 24(b) only compares this work with the other two studies. Among them, the study [**55**] is computational simulation result, while the study [**48**] is chip measurement result. The proposed ED spike detector achieves a comparable FPR values as that of [**48**], but, in terms of power dissipation, it consumes only $\sim$1/10 of the power dissipated by the spike detector reported in [**48**].



(a)



(b)

Figure 24: (a) The comparison of TPR values at different SNR values, (b) The comparison of the FPR values at different SNR values.

Summary of Spike Detectors

This study presents two spike detectors, the fNEO spike detector and the ED spike detector, based on the modified NEO algorithms. The simulation results shown in the study have

demonstrated that both detectors can solve the sensitivity degradation suffered by the conventional NEO spike detectors at the presence of large-amplitude baseline interferences. Among them, we select the ED spike detector for our application due to its extremely low-power performance which is only 129.4 nW. A large amount of statistical investigations have been performed to validate the robustness of the proposed ED spike detector. Considering the low-power and high sensitivity features, the proposed ED spike detector is expected to be a promising data-compression component for an implantable VLSI neural recording microsystem with more than 100 channels.

5. POWER-EFFICIENT TRANSMITTERS

Low-Power Neuromorphic Circuits

Amperometric sensor circuit equipped with floating-gate field-effect transistors (FG-FETs) have been extensively used in environmental and biomedical fields for biomolecular detections. Considering the stringent power and dimension requirements of this type of sensors, here we present a low-power biomolecular sensor circuit designed in the concept of neuromorphic circuits. A silicon neuron based sensor circuit [**64**] is developed to generate a modulated frequency output in response to different current values. The silicon neuron is reconfigured based on a bio-physically inspired neuron model and the proposed circuit achieves nanoampere-level current sensitivity and kilohertz output frequency range. The circuit is designed with a standard 0.13-μm CMOS process. The entire circuit uses only 8 transistors and 4 capacitors and consumes only 2.2 μW power with a 1.1 V supply. The low power dissipation and high area-efficient features of the proposed amperometric sensor circuit make it very suitable for the implanted biomolecular detections.

Introduction of Neuromorphic Circuits

Biomolecular detections are important for both clinical applications and biological studies. The high sensitivity biomolecular detection provides high resolution measurements on the biochemical changes. The new-emerging implanted biomolecular detections have allowed the study of biochemical changes in the tissues of animals when they are behavioring freely, which is significant for the biological studies.

Semiconductor based biosensors have attracted strong interests from researchers in the past decade [**65**]-[**69**]. Owing to its low-cost, high integration, and label-free features, a floating-gate field-effect transistor (FG-FET) based biosensor have been intensively studied for biomolecular detections, such as the detection of electrolytes [**65**], DNA hybridizations

[**66**][**67**], glucose determinations [**68**][**69**], etc. The working principle of this type of sensors can be explained as below: the floating-gate of the FG-FET is capacitively coupled to the sensing area (where biochemical species are adsorbed) and the control-gate [**70**]. As a result, the drain current of the FG-FET is a function of the applied control-gate voltage and the charge on the sensing area. The fluctuations in the amount of biomolecular charges modulate the threshold voltage of the FG-FET and cause a drain current variations at the output. Although this type of sensors can sense the biomolecular charges with high precision, the very small drain current variation, typically in nanoampere level, requires a carefully designed amperometric sensor circuit at its following stage.

Traditional amperometric sensor circuits [**71**][**72**] amplify the very small sensor current to the microampere level and then send it to the analog-to-digital converter (ADC). This strategy increases the system complexity and power dissipation. The other type of amperometric sensor circuits senses the very small current and converts it to the frequency signals. It avoids the use of the current amplifier, sample-and-hold block and ADC blocks, which dramatically reduces the power dissipation of the sensor system.

Biomimetic signal processing circuits have been intensively studied by the researchers to achieve the high energy-efficient signal processing. Multiple neuromorphic silicon neuron circuits [**73**][**74**] have been proposed to build the low-power signal processing systems. Since a silicon neuron circuit can respond to an external current stimulation with different neural spike sequences, here we propose a neuromorphic sensor circuit based on a bio-physical silicon neuron model[**74**]. However, unlike the original model which works at a relatively low frequency range, the silicon neuron circuit developed in this study can generate frequency output up to 11.7 kHz and has nanoampere-level current sensitivity.

Neuromorphic sensor circuit

The overall circuit is shown in Fig. 25. It comprises a FG-FET sensing area, a membrane capacitor C_m, a sodium channel and a potassium channel. The working mechanism of the entire sensor circuit can be illustrated as follows: when the charged molecules appear on

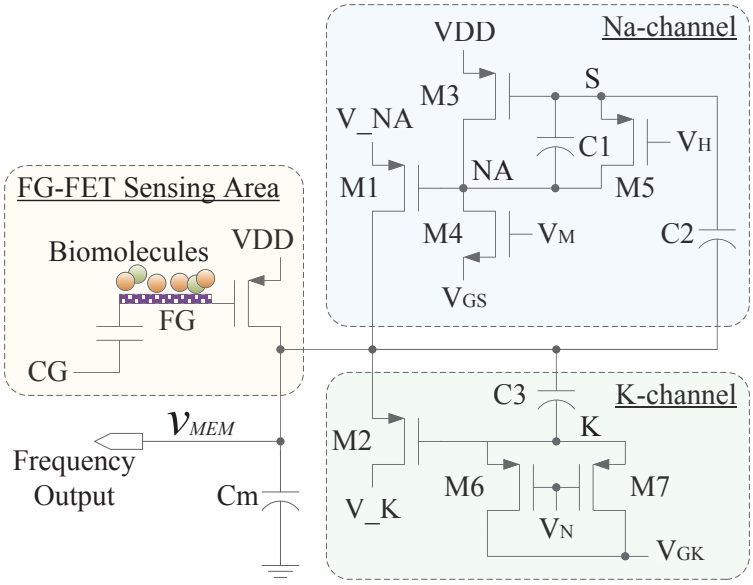


Figure 25: Circuit schematic of the proposed neuromorphic CMOS sensor circuit. (CG: control gate; FG: floating-gate.).

the sensing area, the threshold of the FG-FET is changed. Accordingly, a drain current variation will be produced at the drain terminal of the FG-FET. The silicon neuron based current sensor circuit detects this current changes and then initiates a sequence of spikes on its membrane.

Sodium channel circuit. A sodium channel is responsible for the charging of a cell potential. The step response of a sodium channel is demonstrated to be similar with the output of a bandpass filter [**73**][**74**]. Thus, a sodium channel can be designed with one transistor, the gate of which is controlled by a bandpass filter. As shown in Fig. 25, the proposed silicon neuron based sensor circuit uses one transistor M1 to imitate the functionality of a sodium channel. Transistors M3-M5 and capacitors C1-C2 form the bandpass filter to control the gate of transistor M1. To derive the time constants of the bandpass filter, two working states need to be considered: the low-frequency working state and the high-frequency working state. We can decide the lower cutoff frequency and the higher cutoff frequency of the circuit by analysing the circuit working principle in these two states.

As shown in Fig. 25, when the circuit operates in the low-frequency working state, most of the AC current flowing from node S to node NA is through the transistor M5. The

drain current of transistor M5 can be represented as

$$I_5 = I_{0p}\frac{W_5}{L_5}e^{\frac{\kappa(V_W - V_H)}{U_T}}\left(e^{\frac{-(V_W - v_S)}{U_T}} - e^{\frac{-(V_W - v_{NA})}{U_T}}\right) \tag{5.1}$$

where I_{0p} is a process-dependant constant in the range of $10^{-19} \sim 10^{-14}$ A; κ is the gate coupling coefficient ranging between 0.6 and 0.8; V_W is the well potential; $\frac{W}{L}$ is the device aspect ratio; U_T is the thermal voltage and the typical value is 26 mV @ 300 K. If transistor M5 can sustain a large enough current to maintain the voltage at node S, v_S, constant, v_S can be written as V_S. Since V_S is equal to V_{NA} at the steady state, the equation (5.1) can be rewritten as

$$\begin{aligned} &I_5 = I_{5DC}\left(1 - e^{\frac{v_{na}}{U_T}}\right) \\ &where\ I_{5DC} = I_{0p}\frac{W_5}{L_5}e^{\frac{\kappa(V_W - V_H) - (V_W - V_{NA})}{U_T}} \end{aligned} \tag{5.2}$$

Here, I_{5DC} is decided by the DC bias of transistor M5. v_{na} is the AC signal at node NA. Now, based on KCL, we can write the current function at node S as

$$C_2\frac{d(v_{MEM} - v_S)}{dt} = C_1\frac{d(v_S - v_{NA})}{dt} + I_{5DC}\left(1 - e^{\frac{v_{na}}{U_T}}\right) \tag{5.3}$$

As $v_S = V_S = V_{NA} = constant$, $v_{MEM} = v_{mem} + V_{MEM}$, and $v_{NA} = v_{na} + V_{NA}$, the equation (5.3) can be simplified to

$$C_1\frac{dv_{na}}{dt} = -C_2\frac{dv_{mem}}{dt} - I_{5DC}(e^{\frac{v_{na}}{U_T}} - 1) \tag{5.4}$$

By solving the equation (5.4), the time constant for the lower cutoff frequency can be obtained as

$$\tau_L = \frac{C_1 U_T}{I_{5DC}} \tag{5.5}$$

When the circuit operates in the very-high-frequency working state, capacitive feed-through occurs. The gate-to-source leakage capacitor, C_{gs}, of transistor M1 needs to be considered. By doing the AC analysis on the capacitor loop created by C_2, C_1 and C_{gs}, the

relationship of v_{na}, v_s and v_{mem} can be denoted as

$$v_{na} = \frac{C_1 C_2 v_{mem}}{C_1 C_2 + C_1 C_{gs} + C_2 C_{gs}} \tag{5.6}$$

$$v_s = \frac{(C_1 C_2 + C_2 C_{gs}) v_{mem}}{C_1 C_2 + C_1 C_{gs} + C_2 C_{gs}} \tag{5.7}$$

As the transistor M3 and transistor M4 operate in the weak inversion saturation region, the drain currents can be represented as

$$\begin{aligned} I_3 &= I_{0p} \frac{W_3}{L_3} e^{\frac{\kappa(V_W - (V_S + v_s)) - (V_W - V_{DD})}{U_T}} = I_{3DC} e^{\frac{-\kappa v_s}{U_T}} \\ where\ I_{3DC} &= I_{0p} \frac{W_3}{L_3} e^{\frac{\kappa(V_W - V_S) - (V_W - V_{DD})}{U_T}} \end{aligned} \tag{5.8}$$

$$I_4 = I_{0n} \frac{W_4}{L_4} e^{\frac{\kappa V_M - V_{GS}}{U_T}} = I_{4DC} \tag{5.9}$$

where I_{0n} is a process-dependant constant in the range of $10^{-15} \sim 10^{-12}$ A. Now, we can write the current function at node NA with KCL

$$C_{gs} \frac{dv_{NA}}{dt} + I_{4DC} = I_{3DC} e^{\frac{-\kappa v_s}{U_T}} + C_1 \frac{d(v_S - v_{NA})}{dt} \tag{5.10}$$

As I_{3DC}=I_{4DC} in the steady state, $v_S = v_s + V_S$ and $v_{NA} = v_{na} + V_{NA}$, the equation (5.10) can be simplified to

$$(C_1 + C_{gs}) \frac{dv_{na}}{dt} + I_{4DC} \left(1 - e^{\frac{-\kappa v_s}{U_T}}\right) = C_1 \frac{dv_s}{dt} \tag{5.11}$$

The higher cutoff frequency can be calculated as based on the derivation reported in [**74**]

$$\tau_H = \frac{(C_1 C_2 + C_1 C_{gs} + C_2 C_{gs}) U_T}{\kappa C_1 I_{4DC}} \tag{5.12}$$

From equations (5.5) and (5.12), it can be seen that the lower cutoff frequency and the higher cutoff frequency of the bandpass filter can be tuned by the DC bias currents of the transistors M5 and M4, respectively. In the circuit, the DC voltages V_H and V_M are used to tune the bias currents of transistors M5 and M4, respectively.

Potassium channel circuit. A potassium channel is responsible for the discharging of a cell potential, but has a slower response than a sodium channel. The step response of

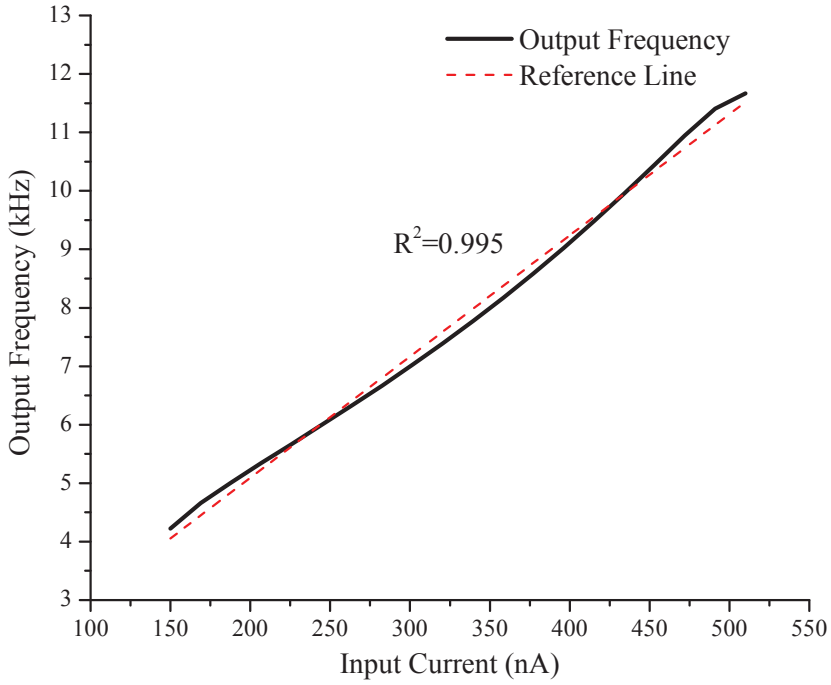


Figure 26: The changes of the output frequency corresponding to the variation of input current.

a potassium channel is similar to the output of a low-pass filter [**73**][**74**]. Therefore, a potassium channel can be designed with one transistor, the gate of which is controlled by a low-pass filter. As shown in Fig. 25, the proposed silicon neuron based sensor circuit uses one transistor M2 to imitate the functionality of a potassium channel. Transistors M6, M7 and capacitor C3 form the low-pass filter to control the gate of transistor M2. Different from the silicon neuron model reported in [**74**], here an additional transistor, M7, is added in the low-pass filter to reduce the time constant.

The time constant of the low-pass filter shown in Fig. 25 is determined by the product of resistance and capacitance seen at node K. By varying the resistance of transistors M6 and M7, the time constant of the low-pass filter can be modified. For a silicon neuron circuit, it is expected that the time constant should be larger for smaller input and smaller for larger ones. The working principle of the low-pass filter circuit shown in Fig. 25 can be described below. When the circuit is in steady state, the potential v_K is equal to bias potential V_{GK}. When a current stimulus is imposed on the membrane capacitor C_m, the membrane potential

increases, which causes the potential at v_K also rising up. For weak inversion pMOSFETs, when the source-to-drain voltage is smaller than $4U_T$, the drain current can be represented as

$$I = I_{0p}\frac{W}{L}e^{\frac{\kappa(V_W - V_N)}{U_T}}\left(e^{\frac{-(V_W - v_K)}{U_T}} - e^{\frac{-(V_W - V_{GK})}{U_T}}\right) \tag{5.13}$$

The conductance of transistors M6 and M7 can be calculated by taking the partial derivative on the equation (5.13) with respect to v_K. The conductance obtained is

$$G_K = \frac{1}{R_K} = I_{0p}\frac{W}{L}\left(\frac{1}{U_T}\right)e^{\frac{\kappa(V_W - V_N)}{U_T}}e^{\frac{-(V_W - v_K)}{U_T}} \tag{5.14}$$

The time constant can be represented as

$$\tau_K = R_K C_K = \frac{C_K}{G_K} \tag{5.15}$$

From equations (5.14) and (5.15), we can notice that a larger v_K causes a larger G_K, which results in a smaller time constant τ, and vice versa. This property is actually what we needed for the current sensing. For larger current, the time constant becomes smaller which leads to the higher frequency output. For smaller current, the time constant becomes larger which corresponds to a lower frequency. In addition, by tuning the DC bias voltage V_N to different values, different initial time constant can be achieved.

Simulation Results

The proposed current sensor circuit is designed using a standard 0.13-μm CMOS process. With a 1.1 V supply, the total power dissipation of the circuit is 2.2 μW. As shown in Fig. 26, when the detected current varies from 150 nA to 510 nA, the frequency of the output neural spikes changes from 4.2 kHz to 11.7 kHz. The coefficient of determination, or R^2, in this range is 0.995. The result indicates a good linearity of the proposed current sensor circuit in response to the variation of the detected current. The root-mean-square

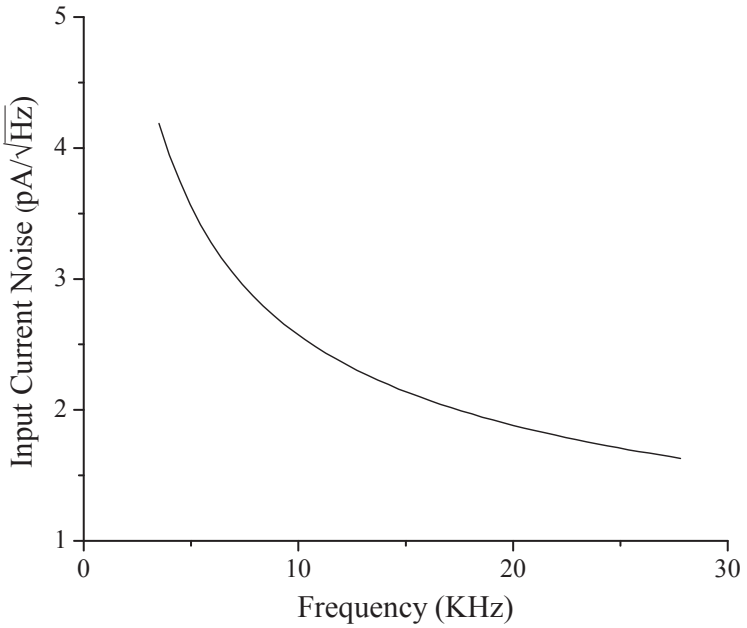


Figure 27: Input current noise from 3.5 kHz to 27.8 kHz.

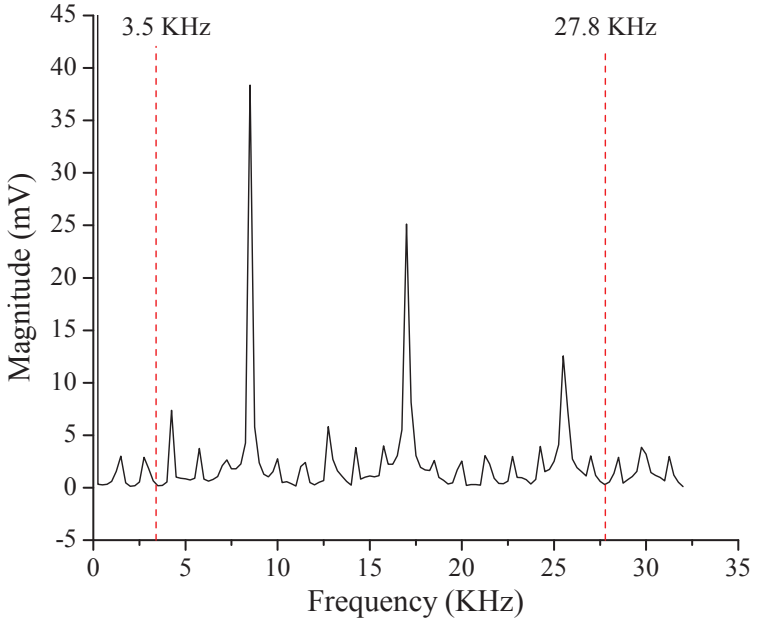


Figure 28: The spectra of the output neural spikes for the 8.5 kHz frequency output.

input-referred noise of the circuit determines the dynamic range and the detection resolution. To show the noise performance of the proposed sensor circuit, the plot of current noise at different frequency is shown in Fig. 27. The plot is drawn when 370 nA current

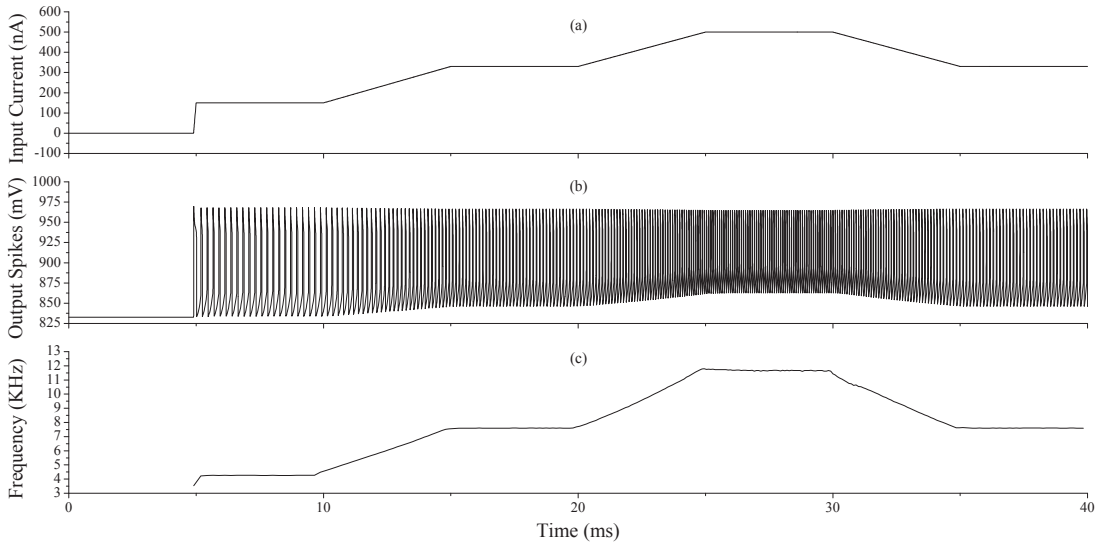


Figure 29: The changes of the output frequency corresponding to the variation of the input current amplitude.

is detected by the circuit, which produces a output neural spike sequence at 8.5 kHz. Fig. 28 exhibits the spectra of the output neural spikes. A noise bandwidth from 3.5 kHz to 27.8 kHz is selected as shown in Fig. 28. Therefore, the calculated input-referred current noise is 0.4 nA_{rms}. The dynamic range of the proposed neuromorphic sensor circuit is 20log10(Irange/Imin)=51 dB. In order to demonstrate the transient response of the proposed circuit, a synthesized current signal (Fig. 29(a)) with steps at 150 nA, 330 nA, and 500 nA is delivered to the circuit. The slop between two steps is $\pm$36 nA/ms. Fig. 29(b) illustrates the output neural spikes of the proposed current sensor circuit in response to the synthesized current signal. To depict the frequency of the output neural spikes, Fig. 29(c) shows the numeric frequency changes calculated from the data shown in Fig. 29(b). By comparing the waveforms of Fig. 29(a) and Fig. 29(c), it is easy to see the close relationship between the input current amplitude and the output frequency.

Summary of Neuromorphic Circuits

Inspired from the biological phenomena that a single neural cell can respond to a current stimulation with different neural spike signals, this study proposes a neuromorphic sensor

circuit which can respond to the current variations with different frequency spike signals. Based on CMOS weak inversion circuit design, a low-power neuromorphic sensor circuit is developed to sense the very small current variations at the output of the FG-FET based biomolecular sensor. The sensor circuit uses a bio-physically inspired silicon neuron model which imitates the membrane potential dynamics caused by a sodium channel and a potassium channel. The frequency output, instead of traditional amplitude output, lowers the complexity of the succeeding signal processing blocks by eliminating multiple signal processing stages, such as current amplification stage, sample and holding stage, etc. Owing to its simple structure (8 MOSFETs and 4 capacitors) and low power dissipation (2.2 μW), the proposed sensor circuit can be easily integrated with different biosensors for the implanted biomolecular detections.

An Inductorless Low-Power Tunable Sinusoidal Oscillator

A sinusoidal oscillator is the stimulation source of a micro-impedance spectroscopy. The accuracy of its output frequency and waveform dictates the accuracy of the measured complex tissue impedance. In this study, an area-efficient low-power sinusoidal oscillator [**75**] is developed for applications requiring low-power high-density bio-impedance measurements. Instead of using traditional LC tank based topology, the proposed sinusoidal oscillator implements a series of hyperbolic tangent functions to approximate the sine function. To achieve the continuous sinusoidal oscillation, a sine waveform shaper, a ramp signal generator, and a fully differential driver are developed for the proposed sinusoidal oscillator. To minimize the power dissipation, a low power supply voltage, 0.5 V, is used in the circuit. Designed in a standard 0.13-μm CMOS process, the proposed sinusoidal oscillator can generate continuous sinusoidal signal with a tuning range of 10 Hz - 4 kHz. It dissipates power of < 3 μW and occupies a die area of 0.07 mm^2.

Bio-impedances of various biological tissues hold significant values in biological studies and clinical evaluations. It helps biologists to understand tissue well-beings. For example, the electrical impedance of a breast tissue has been studied to identify the malignant breast tumors [**76**]. In the past years, many efforts have been made on precise measurements of biological tissues, such as cardiac muscle tissues, lung tissues, mesenteric vessels, and so on.

State of the art impedance spectroscopies usually use four-electrode configuration [**77**] [**78**]. Although both DC and AC (single frequency) sources [**79**] are still widely used, many studies in which the electrical properties of tissues are presumed to be stable have started to use AC source with multiple frequencies [**77**] [**80**]. Micro-impedance spectroscopy using multi-frequency sinusoidal source can measure complex tissue impedances by delivering sinusoidal current signal with multiple different frequencies to the tissue and sensing the voltage variations. With the help of impedance calculation algorithms, the magnitude and phase of the impedance can be calculated. Recently, sinusoidal approximation has been demonstrated to resolve complex impedance spectra from heart preparations [**80**].

Sinusoidal oscillator, or sinusoidal current generator, is one of the most important components in a micro-impedance spectroscopy. The design of this sourcing device needs to meet several main requirements. Firstly, the sinusoidal oscillator must be able to generate a sinusoidal signal with a frequency tuning range of 10 Hz $\sim$ 4 kHz. Secondly, the sinusoidal oscillator needs to supply a current in the range of 10 nA to 50 nA [**80**]. In addition, it is highly desired that the circuit has small dimensions which allows an easy integration with micro-electrodes. However, the design of a small size fully on-chip low-frequency sinusoidal oscillator is challenging in technique level. While traditional ring oscillators or relaxation oscillators can achieve low-frequency oscillation in a small dimensions, neither of them can produce accurate sinusoidal signal. On the other side, although LC oscillators can generate accurate sinusoidal signal, it requires large external inductors in their circuits. Direct Digital Synthesis (DDS) technique can be used to generate a low-distortion

sinusoidal signal with a relatively small circuit size, but the system complexity and power dissipation are increased in this approach. The implementation of a filter based sinusoidal signal generator is limited by the relative low Q value. Numerical analysis on sine function has demonstrated that a set of hyperbolic tangent functions with different phase offsets can be used to approximate a sine function [**81**]. In previous studies, BJT and subthreshold CMOS based differential pairs have been used to implement the sine waveform shapers [**81**][**82**][**83**]. However, these studies have only demonstrated a short piece of sine waveform, instead of a continuous low-distortion sinusoidal signal [**84**][**85**].

In this study, we employed the technique of sine waveform shaper and combined it with a ramp signal generator to build a sinusoidal oscillator. By changing the frequency of the ramp signal, the frequency of the sinusoidal signal can be tuned.

Four-electrode Micro-impedance Spectroscopy

Most of the micro-impedance spectroscopies use four-electrode configuration which provides superior common-mode noise rejection and setup flexibility. As shown in Fig. 30, the four-electrode configuration arranges four electrode E1, E2, E3, and E4 in a line. The two outer-electrodes E1 and E4 are used for current sourcing, while the two inner-electrodes E2 and E3 are used for voltage sensing. When the current flows between the electrodes E1 and E4, different voltages are formed between the electrodes E2 and E3 due to different bio-impedances of the tissues. The electrodes E2 and E3, are set close for a relatively even current flow in the tissues, which can help to reduce the measurement error.

The bio-impedances of tissues are quite different. The resistivity of a tissue decides the values of its bio-impedance. The pioneering research [**86**] has made a detailed study on the resistivities of various tissues. Table 1 summarizes the resistivities of various tissues in terms of the mean values and 95% confidence intervals. From the table, we can see blood has the smallest resistivity, while bone has the largest resistivity. In this study, we target to measure the tissue with resistivity in the range of 100$\sim$500 Ω·cm.

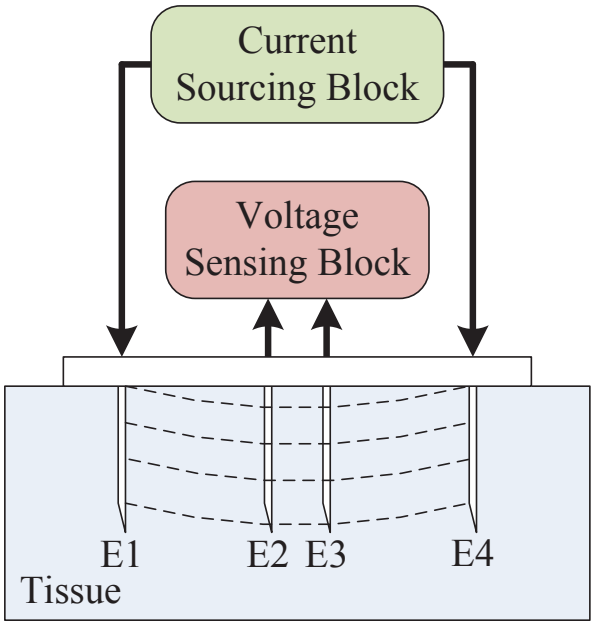


Figure 30: The four-electrode configuration. E1 and E4 are current sourcing electrodes; E2 and E3 are voltage sensing electrodes.

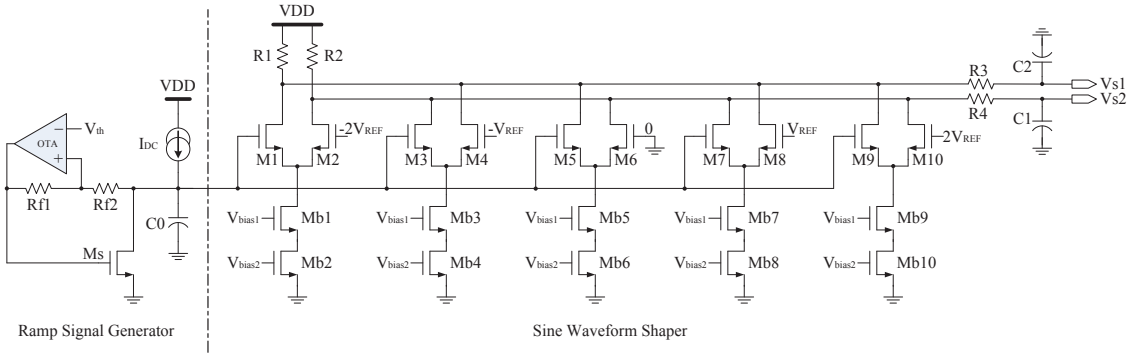


Figure 31: The schematic of the proposed sinusoidal oscillator circuit.

Proposed Sinusoidal Oscillator

The proposed sinusoidal oscillator comprises a sine waveform shaper, a tunable ramp signal generator, and a fully differential driver.

Sine Waveform Shaper. Numerical analysis on sine function has proved that a group of hyperbolic tangent functions with different phase offsets can be used to approximate a sine function [**81**]. Thus, a sine function can be expressed as

$$\beta sin(\frac{\pi x}{\alpha}) \approx \sum_{m=-M}^{M} (-1)^m tanh(x+m\alpha), \text{ if } M \text{ is large.} \tag{5.16}$$

Here, β is an amplitude-scaling constant, while α is a phase offset constant. As the value of M increases, the accuracy of the approximation is improved and finally the approximation fits the sine waveform very closely.

In subthreshold circuit design, the difference of two drain currents in a differential pair is a hyperbolic tangent function of the gate voltages. The relationship can be represented as

$$I_1 - I_2 = I_{bias} \cdot tanh(\frac{V_1 - V_2}{2nU_T}) \tag{5.17}$$

where I_1 and I_2 represent the drain currents in the differential pair, I_{bias} is the tail current, n denotes the slope factor, and U_T is the thermal voltage (26 mV @ 300K).

Based on (5.16) and (5.17), we can design a sine waveform voltage output with a group of subthreshold differential pairs. The mathematical model of the circuit can be expressed as

$$sin(\frac{\pi V_{in}}{V_{REF}}) \approx \sum_{m=-M}^{M} (-1)^m \cdot tanh(\frac{V_{in} + mV_{REF}}{2nU_T}) \tag{5.18}$$

where mV_{REF} are a set of gate bias voltages connected to one of the input gates of each pair. The other gate terminals of the differential pairs are tied together and used as the input terminal. In this design, we select a value of 2 for the variable m. Then, if we take (5.17) into (5.18), we can have the expression as below

$$\begin{aligned} sin(\frac{\pi V_{in}}{V_{REF}}) \approx \frac{1}{I_{bias}} [&(I_{in} - I_{(-2V_{REF})}) - (I_{in} - I_{(-V_{REF})}) \\ &+ (I_{in} - I_{(0)}) - (I_{in} - I_{(V_{REF})}) + (I_{in} - I_{(2V_{REF})})]. \end{aligned} \tag{5.19}$$

Table 6: The resistivities of various tissues presented in terms of the mean values and 95% confidence intervals

Tissue	Water (%)	Mean (Ω·cm)	95% confidence (Ω·cm)
Blood		151	120-191
Bone		124×10^6	91×10^6-169×10^6
Breast		339	249-463
Fat	12.5	3850	3046-4868
Heart		175	133-231
Kidney	78.5	211	160-278
Liver	75	342	296-396
Lung	81.5	157	122-202
Muscle	75.5	171	135-216
Skin	68	329	255-424

From equation (5.19), we can see that five differential pairs are needed to implement the sine waveform shaper. The differential output current of each differential pair needs to have opposite polarity with its neighbors. The implemented circuit of sine waveform shaper is shown in the right of Fig. 31. One of the input gates of each pair is tied together and is connected to the output of the ramp signal generator. The other gate terminals of the differential pairs are connected to five pre-defined bias voltages: $-2V_{REF}$, $-V_{REF}$, 0, V_{REF}, $2V_{REF}$. By changing the frequency of the ramp signal, the frequency of the sinusoidal signal can be tuned.

Capacitors C_1, C_2 and resistors R_3, R_4 form a passive low-pass filter at the output of sine waveform shaper circuit. The function of this low-pass filer is to remove the waveform distortion produced by the abrupt change in the ramp signal.

Ramp Signal Generator. In order to generate a continuous ramp signal, a Schmitt trigger based ramp signal generator is developed. As shown in the left of Fig. 31, a DC current source, I_{DC}, is used to charge a capacitor C_0, which creates the slope of the ramp signal. A large transistor M_S is used to create the discharging path of the capacitor C_0. An operational transconductance amplifier (OTA) based non-inverting Schmitt trigger circuit is employed to provide the control signal at the gate of the transistor M_S. The OTA and two resistors (Rf1,Rf2) form a voltage summer circuit adding a part of the output voltage to the input voltage. This positive feedback creates a rapid ON/OFF switching at the output of the OTA.

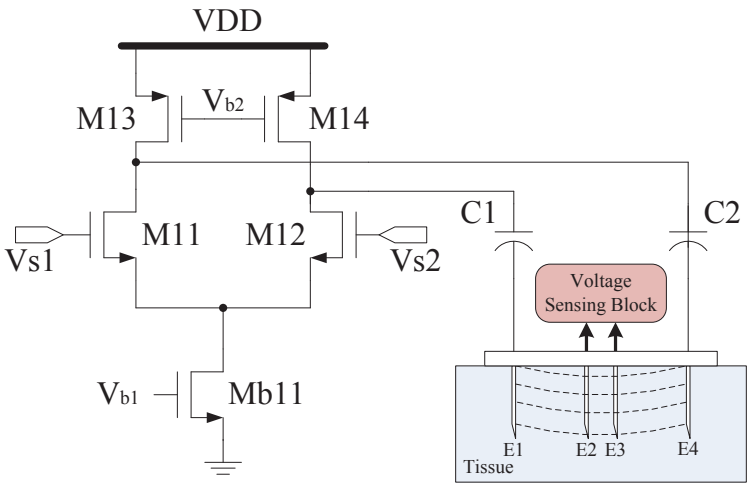


Figure 32: The schematic of the fully differential driver.

If the voltage of the capacitor C_0 is greater than the threshold voltage (V_{th}), the discharging path is turned on and quickly draws the voltage of the capacitor C_0 to zero.

Fully Differential Driver. Since the micro-impedance spectroscopies generally use current signal as the sourcing signal, the sinusoidal voltage signal needs to be converted to current signal. To achieve this conversion, a fully differential amplifier with AC coupling is used to build the driver circuit. It multiplies the differential sinusoidal voltage signal with the transconductance $g_{m11,12}$ and AC couples to the electrodes (E1 and E4). Fig. 32 shows the schematic of the driver circuit. Since the load impedance (bio-impedance) is much smaller than the output impedance of the driver, most of the AC current flows through the capacitors C_1 and C_2 to the load. The output impedance of the driver circuit is 1.25 MΩ. If higher output impedance is demanded, the cascode structure can be applied. However, the cascode stage may require higher power supply voltage which may result in higher power dissipation.

Simulation Results

The proposed circuit has been designed in a standard 0.13-μm CMOS process. With a 0.5 V power supply, the power dissipation of the ramp signal generator, the sinusoidal waveform

shaper, and the fully differential driver are 1.8 μW, 250 nW, and 100 nW, respectively. The driver circuit can provide a stimulation current up to 50 nA which meets the requirement of the study [**80**]. Since no inductor is used in the circuit, the component that mainly impacts the size of the circuit is the capacitor. In this design, three capacitors with decent sizes are used. The capacitor C_0 is 80 pF, while the capacitors C_1 and C_2 are 30 pF. Two resistors (R1 and R2) are 1 MΩ, which can also be realized with active elements and achieve a smaller circuit size. However, the active elements may result in higher noise at the output. The total die area of the proposed sinusoidal oscillator is 0.07 mm^2.

Fig. 33 shows a 2.6 kHz ramp signal generated by the proposed ramp signal generator. By varying the threshold voltage V_{th} in Fig. 31, the amplitude of the output ramp signal can be tuned. However, this variation also changes the frequency of the output ramp signal. In order to tuning the frequency of the output signal without changing its amplitude, we can alter the DC current source I_{DC}. The greater the DC current, the higher the output frequency, and vice versa. By applying the 2.6 kHz ramp signal to the sine waveform shaper, a 2.6 kHz sinusoidal signal can be achieved. The generated 2.6 kHz sinusoidal signal are shown in Fig. 34. Fig. 35 depicts the spectrum profile of the sinusoidal signal shown in Fig. 34. Three peaks in Fig. 35 are the harmonics of the output signal. The first peak is at 2.6 kHz, while the second and third peaks are 5.2 kHz and 7.8 kHz. Fig. 36 shows the phase noise of the output signal at different frequency offset. Phase noise of -79.3 dBc/Hz and -101.4 dBc/Hz can be seen at the frequency offset of 1 Hz and 1 kHz, respectively.

Summary of Sinusoidal Oscillator

In this work, an inductorless low-power tunable sinusoidal oscillator has been developed for micro-impedance spectroscopies. The proposed sinusoidal oscillator comprises a sine

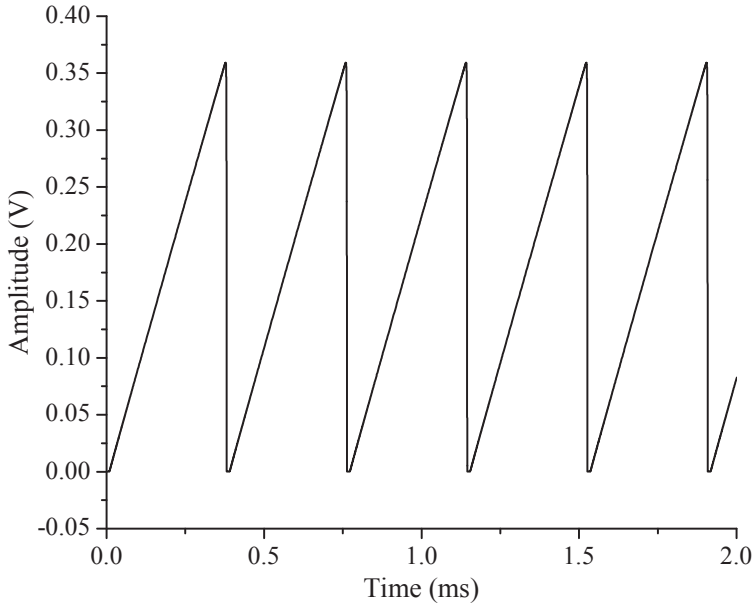


Figure 33: The 2.6 kHz continuous ramp signal generated by the proposed ramp signal generator.

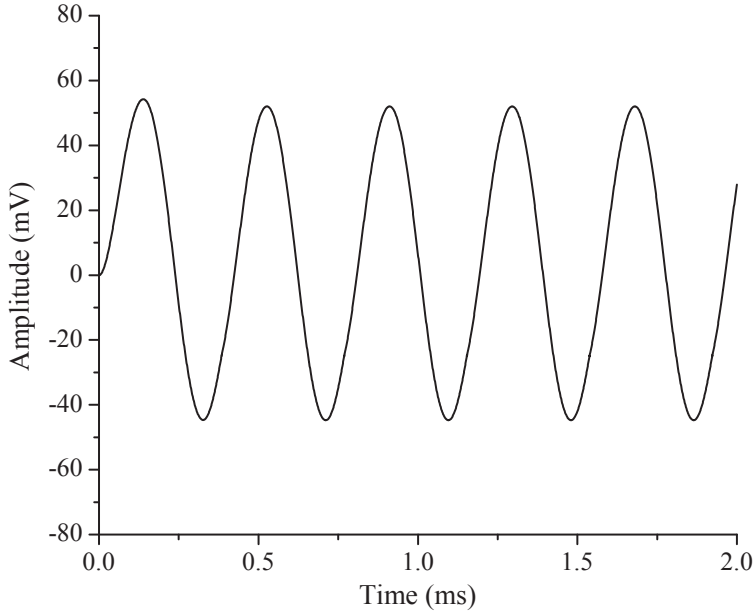


Figure 34: The 2.6 kHz continuous sinusoidal signal generated by the proposed sinusoidal oscillator.

waveform shaper, a ramp signal generator, and a fully differential driver. The sine waveform shaper is built with five subthreshold differential pairs creating five hyperbolic functions to approximate the sine function. The low power dissipation and small dimensions features of the proposed sinusoidal oscillator make it suitable for high-density micro-impedance measurements.

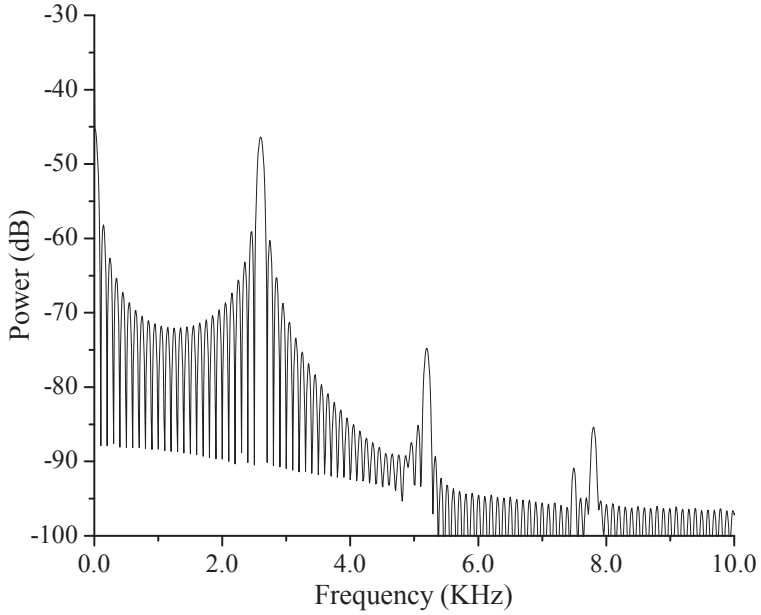


Figure 35: The power spectral density of the 2.6 kHz sinusoidal signal shown in Fig. 34.

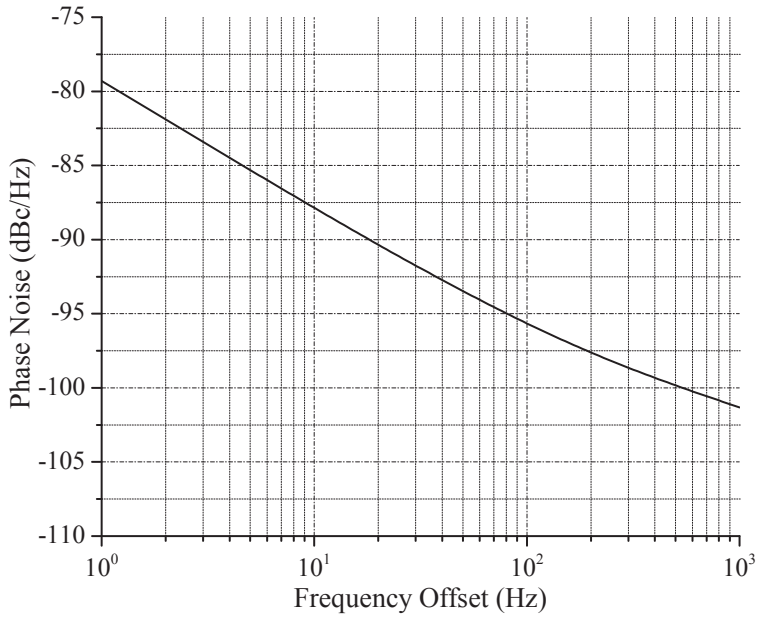


Figure 36: The phase noise of the 2.6 kHz sinusoidal signal shown in Fig. 34.

An Efficient Orthogonal Pulse Set Generator

Due to their orthogonality and the nearly constant pulse width, Modified Hermite Pulses (MHPs) have shown a great potential to enhance the data rate of UWB communications

by creating M-ary or multiple access parallel systems. However, the potential high power dissipation required by the pulse set generation and the frequency shifting has limited their utilization in practice. In this study, we propose a novel computation-efficient model for MHP set generators [**87**]. Compared with existing models, the proposed model has made it feasible to design a power-efficient MHP set generator.

Introduction of Pulse Set Generator

In the field of wireless data acquisition, integration of a large number of recording channels in a small area has become possible owing to the advancement in the fabrication of micro-electromechanical systems (MEMS). However, this increase in the number of recording channels causes a substantial growth in data volume resulting in a big challenge for wireless data transmission [**88**]. For example, a 128-channel recording system with 8-bit resolution working at the Nyquist sampling rate requires a data rate of 20 Mb/s when the target signal is 10 kHz [**5**]. As the number of channels increases, the data rate can rise to 100 Mb/s or higher [**6**]. In order to achieve this data rate, ultra-wideband (UWB) transmission has been widely studied for high-density wireless recordings [**5**][**6**]. However, for applications requiring higher number of channels (e.g. $>$1000) or higher data resolution, an even higher data rate is demanded.

Since orthogonal pulses can be transmitted simultaneously without mutual interference, orthogonal pulses based ultra wideband (UWB) systems have the potential to achieve higher data rate than conventional UWB systems. Several mathematical functions can be used to design UWB orthogonal pulses, such as Haar Function [**89**], Modified Hermite Polynomial Function (MHPF) [**90**][**91**][**92**], Prolate Spheroidal Wave Function (PSWF) [**93**], etc. Each of them has advantages and disadvantages [**94**].

Considering the complicated math model for the generation of orthogonal pulse set, the conventional implementation scheme will be power hungry at the hardware level. As the power dissipation has increasingly attracted attention in modern communication systems, a power-efficient scheme for the generation of orthogonal pulse set is highly desired.

Modified Hermite Pulses (MHPs), which have lower computational complexity than PSWF based pulses, possess the properties of orthogonality and nearly constant pulse widths irrespective of the pulse orders. Since the even order derivatives of MHPs have DC components, additional power is needed for frequency shifting circuits. However, by reducing the range of frequency shifting, lower power dissipation is achievable.

Sub-GHz UWB communications occupy a lower band (0 - 960 MHz) [**23**] than the standard UWB communications (3.1 - 10.6 GHz). The relatively lower frequency spectrum relaxes the system requirements on circuit design, frequency shifting, and communication synchronization, which ultimately reduces the total power dissipation of the system [**95, 96, 97**]. In addition, the sub-GHz UWB pulses have been proven to possess good penetration, low attenuation in air, and little group delay [**23**][**24**]. Although the data rate of a common sub-GHz UWB system is lower than that of a standard UWB system, an orthogonal pulse based sub-GHz UWB system can enhance the data rate by M-ary communications or parallel communications.

In this work, we propose a computation-efficient mathematical model for MHP set generators. A neuromorphic MHP set generator is developed for sub-GHz UWB communications.

Background on Modified Hermite Pulses

The traditional Hermite polynomials can be defined as [**92**]

$$h_{e_n}(t) = (-\tau)^n e^{t^2/2\tau^2} \frac{d^n}{dt^n}\left(e^{-t^2/2\tau^2}\right) \tag{5.20}$$

where $h_{e_n}(t)$ is the nth order derivative of the Hermite polynomial, n is the order of derivative, τ is the time-scale factor, and $t \in (-\infty, \infty)$. The relationship between the nth and the $(n-1)$th order derivatives of Hermite polynomials can be represented as

$$h_{e_{n+1}}(t) = \frac{t}{\tau} h_{e_n}(t) - \tau \dot{h}_{e_n}(t) \tag{5.21}$$

$$\dot{h}_{e_n}(t) = \frac{n}{\tau} h_{e_{n-1}}(t) \tag{5.22}$$

where "$\cdot$" stands for the derivative operation with respect to time. The equations (5.21) and (5.22) can be modified to have only the nth order Hermite polynomials, which can be written as

$$\tau^2 \ddot{h}_{e_n}(t) - t\dot{h}_{e_n}(t) + nh_{e_n}(t) = 0. \tag{5.23}$$

In order to generate orthogonal pulses for UWB communications, MHPs have been proposed and studied by pioneering researchers [**90**][**91**]. The expression of MHPs can be defined as

$$h_n(t) = k_n e^{-t^2/4\tau^2} h_{e_n}(t) \tag{5.24}$$

where $h_{e_n}(t)$ is the nth order derivative of the Hermite polynomial and k_n is a constant related to the energy of the pulse. If we use E_n to denote the energy, the relationship between k_n and E_n can be represented as

$$k_n = \sqrt{\frac{E_n}{\tau n! \sqrt{2\pi}}}. \tag{5.25}$$

By disregarding k_n and taking the equation (5.24) into the equations (5.23), (5.22) and (5.21), the works [**90**][**91**] obtain the general expressions for the nth and the $(n-1)$th order derivatives of MHPs

$$\tau^2 \ddot{h}_n(t) + \left(n + \frac{1}{2} - \frac{1}{4}\frac{t^2}{\tau^2}\right) h_n(t) = 0 \tag{5.26}$$

$$\tau \dot{h}_n(t) + \frac{t}{2\tau} h_n(t) = n h_{n-1}(t) \tag{5.27}$$

$$h_{n+1}(t) = \frac{t}{2\tau} h_n(t) - \tau \dot{h}_n(t). \tag{5.28}$$

In these equations, equation (5.26) contains only the n^{th} order derivative of the MHP. Equations (5.27) and (5.28) reflect the relationships between different order derivatives of MHPs. Based on (5.26) and (5.27), the study [**91**] develops a multiple pulse generator using MATLAB Simulink. In their system, equation (5.26) is firstly implemented to generate the n^{th} order derivative of the MHP. Then, the $(n-1)^{th}$ order derivative of the MHP is produced

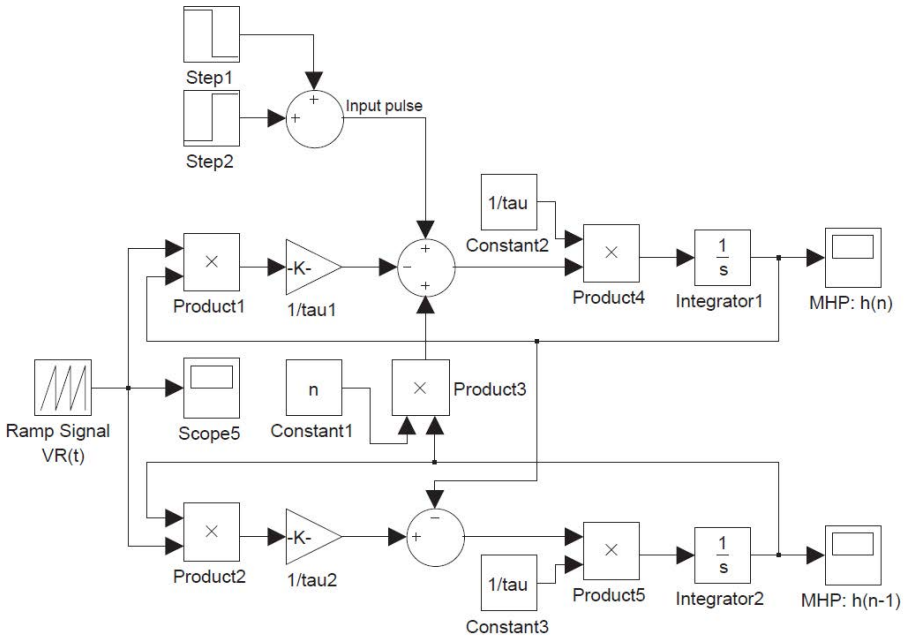


Figure 37: The Simulink block diagram of the proposed computation-efficient MHP set generator.

with equation (5.27). By changing the value of n, different order derivatives of MHPs can be produced.

Proposed Efficient MHP Set Generator

The benefit of using equation (5.26) for MHP generation is that it allows one independent dynamic system to generate one MHP. However, the second order derivative and the squared time function, t^2, make the pulse generator complicated in computation. As shown in the study [**91**], 5 integrators, 8 multipliers and 5 adders are used to generate two different order derivatives of MHPs, implying high power dissipation.

If we replace the n in equation (5.28) with $(n-1)$ and move the derivative terms of equations (5.27) and (5.28) to the left side, the modified equations can be written as

$$\tau\dot{h}_n(t) = -\frac{t}{2\tau}h_n(t) + nh_{n-1}(t) \tag{5.29}$$

$$\tau\dot{h}_{n-1}(t) = \frac{t}{2\tau}h_{n-1}(t) - h_n(t). \tag{5.30}$$

Essentially, equation (5.26) can also be obtained from equations (5.29) and (5.30). However, due to its complicated mathematical operations, equation (5.26) cannot be implemented with an efficient structure. Different from previous studies [**90**][**91**], here we implement equations (5.29) and (5.30) with two interdependent dynamic systems to generate two different order derivatives of MHPs simultaneously. For computational complexity, equation (5.29) has equivalent computational capacity as the equation (5.27), while the equation (5.30) has much lower computational requirements than that of equation (5.26).

The Simulink implementation of equations (5.29) and (5.30) is shown in Fig. 37. Due to our simplified model, there are only 2 integrators, 5 multipliers, 3 adders and a ramp signal generator in the system. Since our goal is to design MHPs for sub-GHz UWB communications, a time-scale factor $\tau = 1 \times 10^{-9}$ is selected to produce MHPs with widths of $\sim$10 ns. Such a width is small enough to guarantee that the pulse spectrum meets the FCC definition of UWB pulses (fractional bandwidth larger than 0.2). Considering the small pulse expansions caused by the higher order derivatives, we have assigned a time-window of 20 ns to ensure the system can generate MHPs up to the 11th order. A ramp signal $V_R(t)$ is employed to substitute the time function $\frac{t}{2}$. For a 20 ns time-window, a ramp signal from 0 nV to 10 nV can be used to represent the time function $\frac{t}{2}$. If the voltage offset is considered, a ramp signal from -5 nV to 5 nV is needed. By varying n to different integers, the impulse responses of two interdependent dynamic systems are the n^{th} and the $(n-1)^{th}$ order derivatives of MHPs. The delivering time-point of the input pulse in the 20 ns time-window can modulate the amplitude of the output MHPs, but the generated pulses are fixed at the middle of the time-window. This feature which is brought by the use of the ramp signal can be explored for pulse amplitude modulation (PAM). Fig. 38 shows four different order derivatives of MHPs generated with the system shown in Fig. 37.

Proposed Neuromorphic MHP Set Generator

In order to achieve a real low-power implementation of the proposed model in practice, an application-specific integrated circuit (ASIC) architecture is needed. Since the left sides of

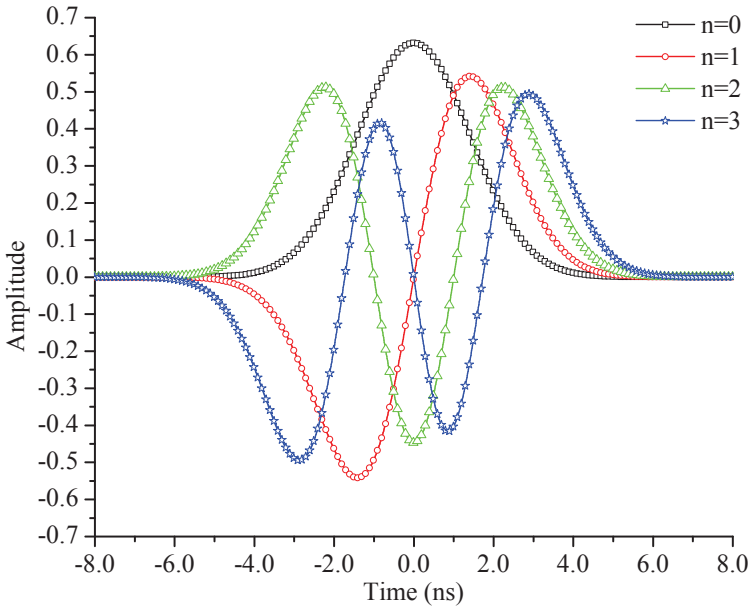


Figure 38: The time responses of the normalized MHPs with n=0, 1, 2, 3. The pulses are normalized for the purpose of display.

equations (5.29) and (5.30) have similar forms as the ion-channel based neuron model, we can utilize silicon neuron circuits to develop the system.

To begin with, two MHP functions, $h_n(t)$ and $h_{n-1}(t)$, can be viewed as the membrane potentials of the silicon neuron n (SiN(n)) and the silicon neuron $(n-1)$ (SiN(n-1)), respectively. As shown in Fig. 39, $h_n(t)$ is represented as the membrane potential of SiN(n), $V_{m(n)}$, while $h_{n-1}(t)$ is represented as the membrane potential of SiN(n-1), $V_{m(n-1)}$. The time-scale factor, τ, is replaced by the membrane capacitor, C_m. As shown in equations (5.29) and (5.30), the left side of each equation becomes the net ion channel current created by the change of membrane potential. The right side of each equation consists of two ion channel currents. The first term is the ion current controlled by the membrane potential of the neuron itself, while the second term is the ion current controlled by the membrane potential of the neighboring neuron. We utilize a self-potential related transconductance, g_s, for the first term and a mutual interactive transconductance, g_m, for the second term. As depicted in Fig. 39, the integer variable n is the number of mutual interactive channels

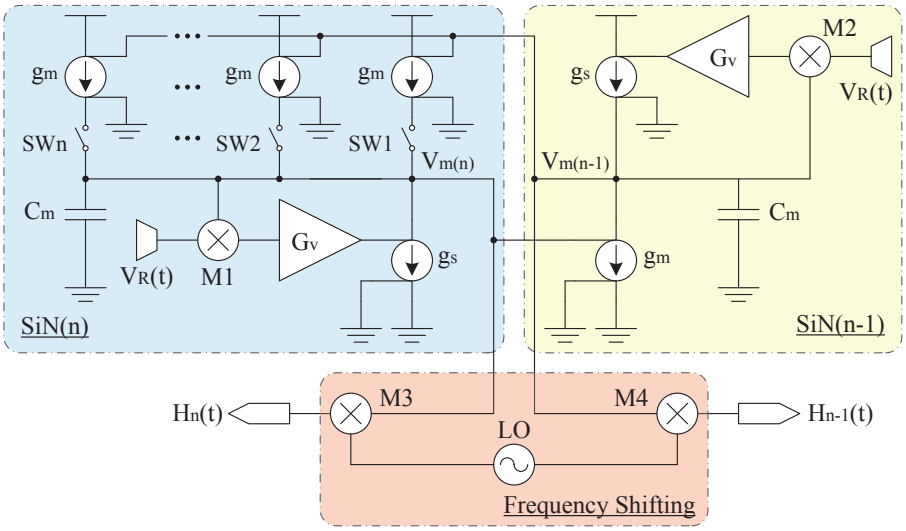


Figure 39: The proposed neuromorphic MHP set generator. SW1-SWn represent the switches used to control the on/off of mutual interactive channels. LO represents a local oscillator with a frequency of 500 MHz. All the biasing circuits are omitted in the figure.

which are controlled by switches. Similar to the Simulink system (Fig. 38), the time function, $\frac{t}{2}$, can be replaced with a ramp signal, $V_R(t)$. Thus, equations (5.29) and (5.30) can be modified into

$$C_m \dot{V}_{m(n)}(t) = -g_s V_R(t) V_{m(n)}(t) + n g_m V_{m(n-1)}(t) \tag{5.31}$$

$$C_m \dot{V}_{m(n-1)}(t) = g_s V_R(t) V_{m(n-1)}(t) - g_m V_{m(n)}(t) \tag{5.32}$$

where C_m is the membrane capacitor of each silicon neuron. $V_{m(n)}$ and $V_{m(n-1)}$ are the membrane potentials of SiN(n) and SiN(n-1), respectively. The symbol g_s is the transconductance related to the membrane potential of the silicon neuron itself, while the symbol g_m is the transconductance related to the mutual interactivity of two neurons. The integer n in the second term of equation (5.31) is the weight of neural interactivity determining the order of derivative of the MHP.

From Fig. 39, we notice that the membrane potential of each silicon neuron is determined by a negative feedback and a positive feedback. For SiN(n), the negative feedback is formed by its membrane potential $V_{m(n)}$, the multiplier $M1$, the gain block G_V, and

the transconductance amplifier g_s. The positive feedback is formed by its membrane potential $V_{m(n)}$, the transconductance amplifier g_m, the membrane potential $V_{m(n-1)}$, and the other transconductance amplifier g_m. Similar feedback loops can also be found in SiN(n-1). Since each silicon neuron generates one MHP, the system shown in Fig. 39 can produce two different order derivatives of MHPs simultaneously. By turning the switches on or off (SW1 $\sim$ SWn), the value of n can be changed, which controls the order of derivative of the MHP. If the application requires multiple different order derivatives of MHPs, a multiplexing strategy can be employed to produce one pair of MHPs at one time slot, or multiple silicon neuron pairs can be implemented in the circuit level for a simultaneous multiple MHPs generation. As shown in the bottom block of Fig. 39, a frequency shifting unit comprising two high-linearity mixers and one 500 MHz oscillator is added to remove the DC components.

To determine the component parameters for the system shown in Fig. 39, we can start with selecting the value for τ. As in the third part, a τ equals to 1×10^{-9} is needed to produce MHPs with the widths around 10 ns, hence a membrane capacitor of 1 nF is needed. Also, since $\frac{t}{2}$ has been replaced by the ramp signal, V_R, which ranges from -5 nV to 5 nV, $\frac{t}{2\tau}$ is in the range of -5 V to 5 V. However, this value is too big for a low-power on-chip design. To solve this problem, we multiply equations (5.31) and (5.32) with a constant, 2×10^{-4}. Consequently, the membrane capacitor, C_m, is scaled down to 200 fF, and the ramp signal is adjusted to the range -1 mV to 1 mV. Considering the values for the self-potential related transconductances in equations (5.31) and (5.32), we finally applied a ramp signal, V_R, ranging from -50 mV to 50 mV, a self-potential related transconductance of 500 μA/V and a voltage amplification gain G_V = 40. Lastly, the system can be modeled as

$$C_m \dot{V}_{m(n)}(t) = -g_s G_V V_R(t) V_{m(n)}(t) + n g_m V_{m(n)}(t) \tag{5.33}$$

$$C_m \dot{V}_{m(n-1)}(t) = g_s G_V V_R(t) V_{m(n-1)}(t) - g_m V_{m(n-1)}(t) \tag{5.34}$$

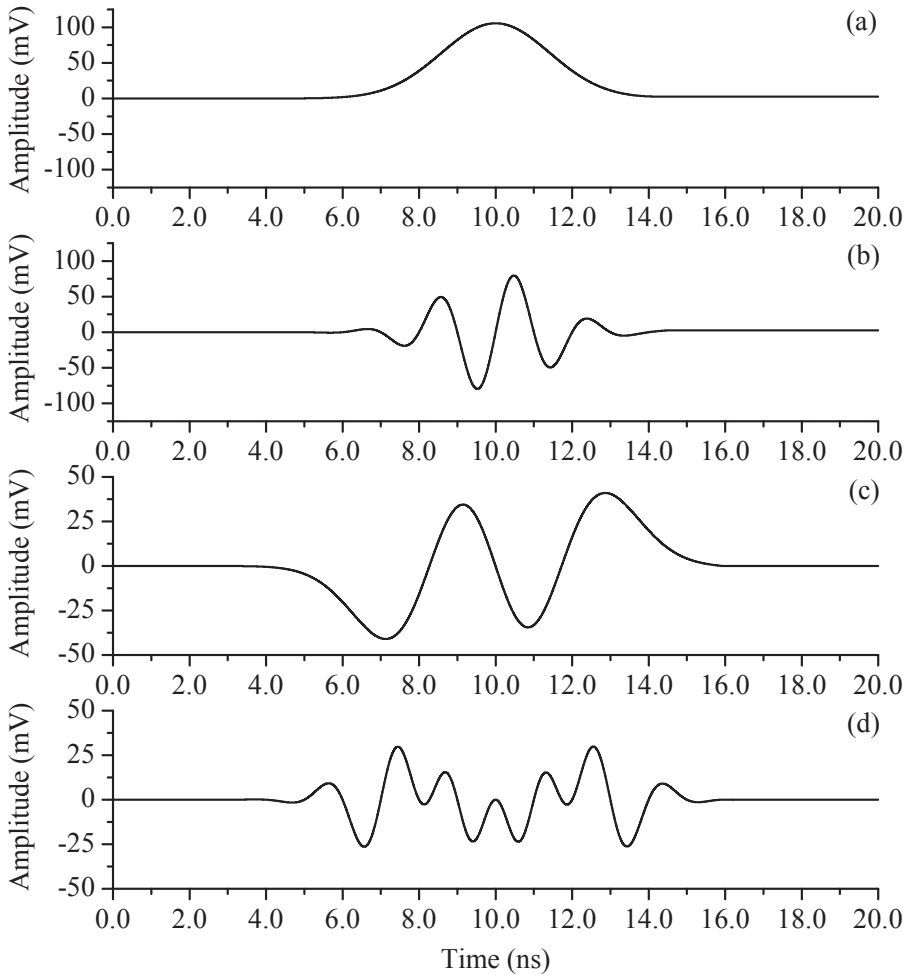


Figure 40: The simulation results of the proposed MHP set generator. (a) The zero order derivative of the MHP, (b) The zero order derivative of the MHP after 500 MHz frequency shifting, (c) The third order derivative of the MHP, (d) The third order derivative of the MHP after 500 MHz frequency shifting.

where

$$C_m = 200\ fF$$

$$g_s = 500\ \mu A/V,\ g_m = 200\ \mu A/V$$

$$G_V = 40,\ V_R = Ramp[-50\ mV, 50\ mV].$$

With the aid of Verilog-AMS, the proposed neuromorphic MHP set generator has been implemented in Cadence. By changing the number of turning-on switches in Fig. 39 from 1 to 4, four different order derivatives of MHPs can be generated. In these four pulses, the

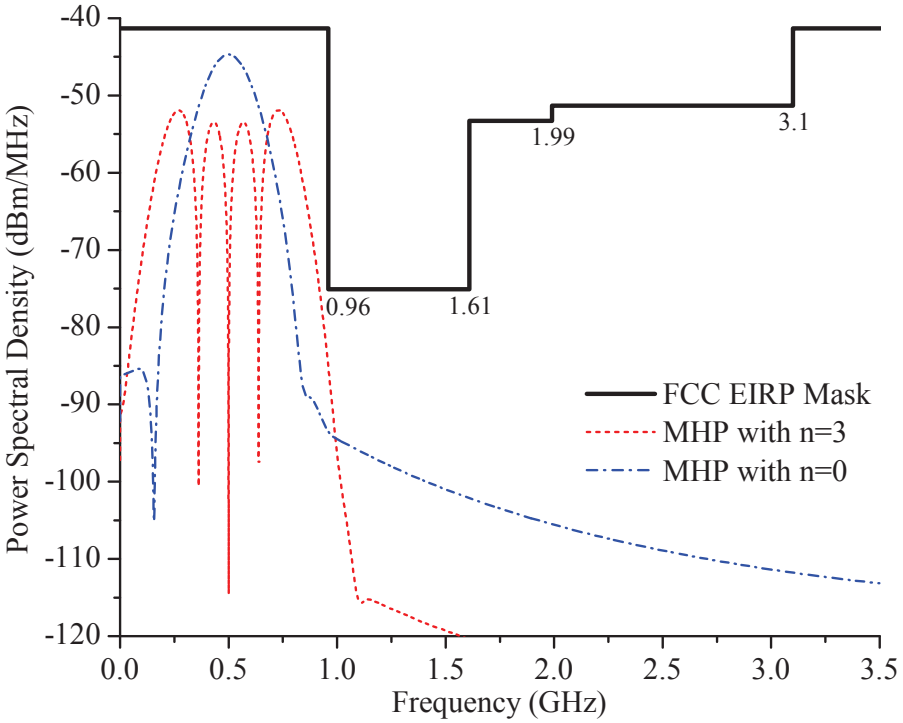


Figure 41: The power spectral density of the generated the zero order and the third order derivatives of MHPs after 500 MHz frequency shifting.

zero order derivative of the MHP has the highest peak, while the third order derivative of the MHP has the largest pulse width. These two waveforms are shown in Fig. 40(a) and Fig. 40(c), respectively. The results exhibit a 10.1 ns width for the zero order derivative of the MHP and a 13.2 ns width for the third order derivative of the MHP. With a 500 MHz frequency shifting, the corresponding modulated MHPs are shown in Fig. 40(b) and Fig. 40(d), respectively. Without considering the antenna gain, the power spectral density of the modulated MHPs is plotted in Fig. 41. Both of them are below the FCC Equivalent Isotropically Radiated Power (EIRP) mask for indoor UWB communications.

Summary of Pulse Set Generator

In this study, we propose an efficient mathematical model for MHP set generators. Compared with existing models, the proposed model has lower computational complexity. For circuit level implementations, a neuromorphic circuit architecture has been developed to

generate MHPs for sub-GHz UWB communications. While the sub-GHz UWB communication allows lower power dissipation than the standard UWB communications, the neuromorphic structure further reduces the numbers of adders, integrators and multipliers needed in the system. Results from both mathematical analysis and design layout simulations validate the effectiveness of the proposed scheme for the design of an efficient MHP set generator.

6. CONCLUSIONS

In this dissertation research, the author has made a complete study on the low-power multichannel telemetry system for high-speed wireless neural recordings. This study covers research works in three main aspects: (1) the investigation of low-power low-noise biosignal amplifiers, (2) the algorithm study and circuit development of neural spike detector, and (3) the transmitter architecture study and neuromorphic circuit research.

In the study of biosignal amplifier, three amplifiers are designed. One is the Ultra-low-power bioamplifier. In this study, the author propose a power and noise efficient bioamplifier for large array biopotential recording systems. The proposed bioamplifier utilizes a differential folded-cascode gain stage and a common-gate gain stage to amplify the biological signal. The wide-swing-cascode structure is employed to achieve high gain under low-voltage low-power operation. Subthreshold region operation of MOSFETs are utilized and the corresponding device dimensions are optimized by extensive computer simulations. The optimum trade-off of power, noise and device dimensions results in an ultra-low-power biosignal amplifier. The proposed bioamplifier is designed using 0.13 μm standard CMOS process. Monte Carlo simulation is performed to validate the system performance with respect to device dimension mismatch. The second amplifier is Low-noise gain-tunable amplifier. In this work, the author presents a gain-tunable biopotential amplifier that achieves an input-referred noise of 4.3 μV_{rms} with 732 nW power consumption. The self-biasing arrangement consisted of weak inversion MOSFETs is demonstrated to achieve the low-noise and low-power amplification. The precisely tunable gain of the proposed amplifier can maximally utilize the resolution of an analog-to-digital converter (ADC) by adjusting the amplitude of the amplified signal to the suited range. The third amplifier is the low-power amplifier with optimized noise efficient factor. The author proposes a low-noise biopotential amplifier with an NEF value close to the theoretical limit of the proposed circuit structure. The NEF theoretical limit of the proposed circuit topology is derived out

first to guide the circuit design process. Based on this NEF value, we calculate the total current needed to achieve the highest power-noise efficiency. The very low input-referred noise is achieved by increasing the transconductance of the input nMOSFET pair. Three approaches are adopted here. Firstly, the nMOSFET pair are biased to operate at weak inversion saturation region for the high transconductance efficiency (g_m/I_D). Secondly, 1/3 of the total current is assigned to the nMOSFET pair. Thirdly, a self-biased structure comprising a weak positive feedback and a strong negative feedback is applied on the circuit to further enhance the transconductance.

In the study of neural spike detectors, the author has shown the sensitivity degradation of conventional NEO spike detectors at the presence of LFPs. We extended our previous work by incorporating a comprehensive evaluation on the detection accuracy of the proposed spike detectors. In second part, the characteristics of three mostly used spike detection algorithms are introduced briefly. The third part elaborates the principles of the proposed spike detection algorithms, namely frequency-enhanced NEO (fNEO) and energy-of-derivative (ED), and compares them with NEO method. In the fourth part, the NEO, fNEO, and ED algorithms are implemented into three low-power full-analog spike detectors and the performance of the proposed algorithms are verified with the implemented spike detectors. A large amount of statistical evaluations have been made in the fifth part to demonstrate the detection robustness of the proposed ED spike detector at different signal-to-noise ratio (SNR). Finally, we conclude this work in the last.

In the study of power-efficient transmitter, we propose an efficient mathematical model for MHP set generators. Compared with existing models, the proposed model has lower computational complexity. For circuit level implementations, a neuromorphic circuit architecture has been developed to generate MHPs for sub-GHz UWB communications. While the sub-GHz UWB communication allows lower power dissipation than the standard UWB communications, the neuromorphic structure further reduces the numbers of adders, integrators and multipliers needed in the system. Results from both mathematical analysis and

design layout simulations validate the effectiveness of the proposed scheme for the design of an efficient MHP set generator.

Bibliography

[1] N. C. Rowland, J. Breshears, and E. F. Chang, "Neurosurgery and the dawning age of brain-machine interfaces," in *SNI: Neurosurgical Developments on the Horizon*, vol. 4, Mar. 2013.

[2] R. Harrison and C. Charles, "A low-power low-noise cmos amplifier for neural recording applications," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 6, pp. 958 – 965, june 2003.

[3] B. Gosselin, M. Sawan, and C. Chapman, "A low-power integrated bioamplifier with active low-frequency suppression," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 1, no. 3, pp. 184 –192, sept. 2007.

[4] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 1, no. 2, pp. 136 –147, june 2007.

[5] M.-S. Chae, Z. Yang, M. Yuce, L. Hoang, and W. Liu, "A 128-channel 6 mw wireless neural recording ic with spike feature extraction and uwb transmitter," *Neural Systems and Rehabilitation Engineering, IEEE Transactions on*, vol. 17, no. 4, pp. 312–321, 2009.

[6] M. Yuce, H. C. Keong, and M. S. Chae, "Wideband communication for implantable and wearable systems," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 57, no. 10, pp. 2597–2604, 2009.

[7] J. Holleman and B. Otis, "A sub-microwatt low-noise amplifier for neural recording," in *Engineering in Medicine and Biology Society, 2007. EMBS 2007. 29th Annual International Conference of the IEEE*, aug. 2007, pp. 3930 –3933.

[8] M. Chae, J. Kim, and W. Liu, "Fully-differential self-biased bio-potential amplifier," *Electronics Letters*, vol. 44, no. 24, pp. 1390–1391, 2008.

[9] J. Kim, M. S. Chae, and W. Liu, "A 220nw neural amplifier for multi-channel neural recording systems," in *Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on*, may 2009, pp. 1257 – 1260.

[10] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor, "Micropower cmos integrated low-noise amplification, filtering, and digitization of multimodal neuropotentials," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 3, no. 1, pp. 1 –10, feb. 2009.

[11] V. Majidzadeh, A. Schmid, and Y. Leblebici, "Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 5, no. 3, pp. 262 –271, june 2011.

[12] V. Chaturvedi and B. Amrutur, "An area-efficient noise-adaptive neural amplifier in 130 nm cmos technology," *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on*, vol. 1, no. 4, pp. 536 –545, dec. 2011.

[13] F. Zhang, J. Holleman, and B. Otis, "Design of ultra-low power biopotential amplifiers for biosignal acquisition applications," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 6, no. 4, pp. 344 –355, aug. 2012.

[14] H. Semmaoui, J. Drolet, A. Lakhssassi, and M. Sawan, "A new approach for higher data reduction capacity based on spike detection technique in wireless multichannel neural recordings," in *Biomedical Engineering Conference (CIBEC), 2010 5th Cairo International*, dec. 2010, pp. 154–157.

[15] A. Kamboh and A. Mason, "On-chip feature extraction for spike sorting in high density implantable neural recording systems," in *Biomedical Circuits and Systems Conference (BioCAS), 2010 IEEE*, Nov. 2010.

[16] Z. Yang, Q. Zhao, and W. Liu, "Improving spike separation using waveform derivatives," *Neural Eng., Journal of*, vol. 6, no. 4, p. 046006, Aug. 2009.

[17] S. Gibson, J. Judy, and D. Markovic, "Technology-aware algorithm design for neural spike detection, feature extraction, and dimensionality reduction," *Neural Systems and Rehabilitation Engineering, IEEE Transactions on*, vol. 18, no. 5, pp. 469 –478, Oct. 2010.

[18] H. Li and Q. Xu, "Sub-threshold-based ultra-low-power neural spike detector," *Electronics Letters*, vol. 47, no. 6, pp. 367 –368, 17 2011.

[19] J. Holleman, A. Mishra, C. Diorio, and B. Otis, "A micro-power neural spike detector and feature extractor in .13 um cmos," in *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, Sept. 2008.

[20] B. Gosselin and M. Sawan, "An ultra low-power cmos automatic action potential detector," *Neural Systems and Rehabilitation Engineering, IEEE Transactions on*, vol. 17, no. 4, pp. 346 –353, Aug. 2009.

[21] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor, "Micropower cmos integrated low-noise amplification, filtering, and digitization of multimodal neuropotentials," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 3, no. 1, pp. 1 –10, feb. 2009.

[22] X. Liu, H. Hao, L. Yang, L. Li, J. Zhang, A. Yang, and Y. Ma, "Epileptic seizure detection with the local field potential of anterior thalamic of rats aiming at real time application," in *Engineering in Medicine and Biology Society,EMBC, 2011 Annual International Conference of the IEEE*, 2011.

[23] Y. Joo, H. Kim, and S. Jung, "A tunable pulse generator for sub-ghz uwb systems," in *Circuits and Systems, 2009. MWSCAS '09. 52nd IEEE International Midwest Symposium on*, 2009, pp. 292–296.

[24] M. Stoopman and A. Wouter, "Sub-ghz uwb biomedical communication," in *Biomedical Circuits and Systems Conference (BioCAS), 2010 IEEE*, 2010, pp. 25–28.

[25] Y.-G. Li, Q. Ma, M. Haider, and Y. Massoud, "An ultra-low-power bioamplifier for implantable large-scale recording of neural activity," in *Wireless and Microwave Technology Conference (WAMICON), 2013 IEEE 14th Annual*, 2013, pp. 1–4.

[26] B. Gosselin, M. Sawan, and C. Chapman, "A low-power integrated bioamplifier with active low-frequency suppression," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 1, no. 3, pp. 184 –192, sept. 2007.

[27] B. Gosselin and M. Sawan, "An ultra low-power cmos automatic action potential detector," *Neural Systems and Rehabilitation Engineering, IEEE Transactions on*, vol. 17, no. 4, pp. 346 –353, aug. 2009.

[28] Y.-G. Li, M. Haider, and Y. Massoud, "A low-noise gain-tunable amplifier for large array biopotential recording systems," *Analog Integrated Circuits and Signal Processing*, vol. 74, no. 2, pp. 485–489, 2013.

[29] J. G. Webster, *Medical Instrumentation Application and Design*, 4th ed. Wiley Press, 2009.

[30] T. M. Seese, H. Harasaki, G. M. Saidel, and C. R. Davies, "Characterization of tissue morphology, angiogenesis, and temperature in the adaptive response of muscle tissue to chronic heating," *Lab. Invest.*, vol. 78, no. 12, pp. 1553–1562, 1998.

[31] L. Liu, X. Zou, W. Goh, R. Ramamoorthy, G. Dawe, and M. Je, "800 nW 43 nV/$\sqrt{\text{Hz}}$ neural recording amplifier with enhanced noise efficiency factor," *Electronics Letters*, vol. 48, no. 9, pp. 479–480, 26 2012.

[32] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical mos transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 83–114, July 1995.

[33] PhysioNet and PhysioBank. (2011, Dec.) Shhs polysomnography database @ONLINE. [Online]. Available: http://physionet.org/physiobank/database/shhpsgdb/

[34] I. A. Kazerouni, H. G. Dehrizi, S. M. M. Isfahani, Z. Zhuo, M. Baghaei-Nejad, and L. R. Zheng, "A 77 nw bioamplifier with a tunable bandwidth for neural recording systems," in *IEEE Asia Pacific Conference on Circuits and Systems*, Dec. 2010, pp. 36–39.

[35] R. Harrison, "The design of integrated circuits to observe brain activity," *Proceedings of the IEEE*, vol. 96, no. 7, pp. 1203 –1216, july 2008.

[36] W. Zhao, H. Li, and Y. Zhang, "A low-noise integrated bioamplifier with active dc offset suppression," in *Biomedical Circuits and Systems Conference, 2009. BioCAS 2009. IEEE*, 2009, pp. 5–8.

[37] C. Liu, J. Chang, S. Yuan, L. Johnson, and R. Rennaker, "A low noise bandpass neuro-amplifier with adjustable bandwidth for bio-medical applications," in *Green Circuits and Systems (ICGCS), 2010 International Conference on*, 2010, pp. 438–441.

[38] S. Saberhosseini, A. Zabihian, and A. Sodagar, "Low-noise ota for neural amplifying applications," in *Devices, Circuits and Systems (ICCDCS), 2012 8th International Caribbean Conference on*, 2012, pp. 1–4.

[39] M. ElGuindy and A. Madian, "Low voltage digitally programmable gain and bandwidth fully differential cmos neural amplifier," in *Biomedical Robotics and Biomechatronics (BioRob), 2012 4th IEEE RAS EMBS International Conference on*, 2012, pp. 477–481.

[40] J. Alexander, M. Lakshmi, and M. Renuga, "Low power eng signal acquisition amplifier for epileptic seizure prediction," in *Electrical, Electronics and Computer Science (SCEECS), 2012 IEEE Students' Conference on*, 2012, pp. 1–4.

[41] S. Saberhosseini, "A micro-power low-noise amplifier for neural recording microsystems," in *Electrical Engineering (ICEE), 2012 20th Iranian Conference on*, 2012, pp. 314–317.

[42] B. Thanigaivelan, J. Wiles, and T. Hamilton, "A low power neural recording amplifier with programmable gain and bandwidth," in *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on*, 2012, pp. 2219–2222.

[43] U. Bihr and M. Ortmanns, "A front-end circuit with active spike and lfp separation via a switched capacitor filter structure for neural recording applications," in *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on*, 2012, pp. 2231–2234.

[44] Y.-G. Li, Q. Ma, M. Haider, and Y. Massoud, "Ultra-low-power high sensitivity spike detectors based on modified nonlinear energy operator," in *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on*, 2013, pp. 137–140.

[45] Y.-G. Li, Y. Massoud, and M. Haider, "Low-power high-sensitivity spike detectors for implantable vlsi neural recording microsystems," *Analog Integrated Circuits and Signal Processing*, vol. 80, no. 3, pp. 449–457, 2014.

[46] R. R. Harrison, P. T. Watkins, R. J. Kier, R. O. Lovejoy, D. J. Black, B. Greger, and F. Solzbacher, "A low-power integrated circuit for a wireless 100-electrode neural recording system," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 1, pp. 123 –133, Jan. 2007.

[47] M.-S. Chae, Z. Yang, M. Yuce, L. Hoang, and W. Liu, "A 128-channel 6 mw wireless neural recording ic with spike feature extraction and uwb transmitter," *Neural Systems and Rehabilitation Engineering, IEEE Transactions on*, vol. 17, no. 4, pp. 312–321, 2009.

[48] A. Rodriguez-Perez, J. Ruiz-Amaya, M. Delgado-Restituto, and A. Rodriguez-Vazquez, "A low-power programmable neural spike detection channel with embedded calibration and data compression," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 6, no. 2, pp. 87 –100, april 2012.

[49] H. Semmaoui, J. Drolet, A. Lakhssassi, and M. Sawan, "A new approach for higher data reduction capacity based on spike detection technique in wireless multichannel neural recordings," in *Biomedical Engineering Conference (CIBEC), 2010 5th Cairo International*, Dec. 2010.

[50] S. Hiseni, C. Sawigun, W. Ngamkham, and W. Serdijn, "A compact, nano-power cmos action potential detector," in *Biomedical Circuits and Systems Conference, 2009. BioCAS 2009. IEEE*, nov. 2009, pp. 97 –100.

[51] S. Barati and A. Sodagar, "Discrete-time automatic spike detection circuit for neural recording implants," *Electronics Letters*, vol. 47, no. 5, pp. 306–307, 2011.

[52] Z. Yang, Q. Zhao, and W. Liu, "Improving spike separation using waveform derivatives," *Neural Eng., Journal of*, vol. 6, no. 4, p. 046006, Aug. 2009.

[53] A. Sarje and P. Abshire, "Low power cmos circuit for spike detection," in *Sensors, 2011 IEEE*, oct. 2011, pp. 928 –931.

[54] J. Kaiser, "On a simple algorithm to calculate the 'energy' of a signal," in *Acoustics, Speech, and Signal Processing, 1990. ICASSP-90., 1990 International Conference on*, 1990, pp. 381–384 vol.1.

[55] S. Gibson, J. Judy, and D. Markovic, "Technology-aware algorithm design for neural spike detection, feature extraction, and dimensionality reduction," *Neural Systems and Rehabilitation Engineering, IEEE Transactions on*, vol. 18, no. 5, pp. 469 –478, oct. 2010.

[56] H. Li and Q. Xu, "Sub-threshold-based ultra-low-power neural spike detector," *Electronics Letters*, vol. 47, no. 6, pp. 367 –368, 17 2011.

[57] J. Holleman, A. Mishra, C. Diorio, and B. Otis, "A micro-power neural spike detector and feature extractor in .13 um cmos," in *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, sept. 2008, pp. 333 –336.

[58] B. Gosselin and M. Sawan, "An ultra low-power cmos automatic action potential detector," *Neural Systems and Rehabilitation Engineering, IEEE Transactions on*, vol. 17, no. 4, pp. 346 –353, aug. 2009.

[59] H. Semmaoui, J. Drolet, A. Lakhssassi, and M. Sawan, "Setting adaptive spike detection threshold for smoothed teo based on robust statistics theory," *Biomedical Engineering, IEEE Transactions on*, vol. 59, no. 2, pp. 474 –482, feb. 2012.

[60] X. Liu, H. Hao, L. Yang, L. Li, J. Zhang, A. Yang, and Y. Ma, "Epileptic seizure detection with the local field potential of anterior thalamic of rats aiming at real time application," in *Engineering in Medicine and Biology Society,EMBC, 2011 Annual International Conference of the IEEE*, 2011.

[61] S. Hiseni, C. Sawigun, and W. Serdijn, "Dynamic translinear nonlinear energy operator," in *Circuit Theory and Design, 2009. ECCTD 2009. European Conference on*, 2009, pp. 153–156.

[62] W. Liu and S.-I. Liu, "Design of a cmos low-power and low-voltage four-quadrant analog multiplier," in *Analog Integr Circ Sig Process*, vol. 63, no. 2, 2010, pp. 307 –312.

[63] A. Singireddy, K. McMillan, and D. Graham, "Compact and low-power continuous-time derivative circuit," *Electronics Letters*, vol. 47, no. 17, pp. 956 –957, 18 2011.

[64] Y.-G. Li and M. Haider, "A low-power neuromorphic cmos sensor circuit for the implanted biomolecular detections," in *SENSORS, 2013 IEEE*, Nov 2013, pp. 1–4.

[65] N.-M. Shen, Z. Liu, C. Lee, B. Minch, and E.-C. Kan, "Charge-based chemical sensors: a neuromorphic approach with chemoreceptive neuron mos (c nu;mos) transistors," *Electron Devices, IEEE Transactions on*, vol. 50, no. 10, pp. 2171–2178, 2003.

[66] M. Barbaro, A. Bonfiglio, and L. Raffo, "A charge-modulated fet for detection of biomolecular processes: conception, modeling, and simulation," *Electron Devices, IEEE Transactions on*, vol. 53, no. 1, pp. 158–166, 2006.

[67] M. Barbaro, A. Bonfiglio, L. Raffo, A. Alessandrini, P. Facci, and I. BarakBarak, "A cmos, fully integrated sensor for electronic detection of dna hybridization," *Electron Device Letters, IEEE*, vol. 27, no. 7, pp. 595–597, 2006.

[68] W.-Y. Chung, A. Paglinawan, Y.-H. Wang, and T.-T. Kuo, "A 600 μw readout circuit with potentiostat for amperometric chemical sensors and glucose meter applications," in *Electron Devices and Solid-State Circuits, 2007. EDSSC 2007. IEEE Conference on*, 2007, pp. 1087–1090.

[69] E. Ekanayake, D. M. G. Preethichandra, and K. Kaneto, "An amperometric glucose biosensor with enhanced measurement stability and sensitivity using an artificially porous conducting polymer," *Instrumentation and Measurement, IEEE Transactions on*, vol. 57, no. 8, pp. 1621–1626, 2008.

[70] B. Chen, A. Parashar, and S. Pandey, "Folded floating-gate cmos biosensor for the detection of charged biochemical molecules," *Sensors Journal, IEEE*, vol. 11, no. 11, pp. 2906–2910, 2011.

[71] A. Bandyopadhyay, G. Mulliken, G. Cauwenberghs, and N. Thakor, "Vlsi potentiostat array for distributed electrochemical neural recording," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, vol. 2, 2002, pp. II–740–II–743 vol.2.

[72] A. Frey, M. Jenkner, M. Schienle, C. Paulus, B. Holzapfl, P. Schindler-Bauer, F. Hofmann, D. Kuhlmeier, J. Krause, J. Albers, W. Gumbrecht, D. Schmitt-Landsiedel, and R. Thewes, "Design of an integrated

potentiostat circuit for cmos bio sensor chips," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 5, 2003, pp. V–9–V–12 vol.5.

[73] A. Hodgkin and A. Huxley, "A quantitative description of membrane current and its application to conduction and excitation in nerve," *J. Physiol.*, vol. 117, pp. 500–544, 1952.

[74] E. Farquhar and P. Hasler, "A bio-physically inspired silicon neuron," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, no. 3, pp. 477–488, 2005.

[75] Y.-G. Li, A. Arifuzzman, A. Pollard, and M. Haider, "An inductorless low-power tunable sinusoidal oscillator for micro-impedance spectroscopy," in *Wireless and Microwave Technology Conference (WAMICON), 2014 IEEE 15th Annual*, June 2014, pp. 1–4.

[76] Y. Zou and Z. Guo, "A review of electrical impedance techniques for breast cancer detection," *Medical Engineering Physics*, vol. 25, no. 2, pp. 79–90, Mar. 2003.

[77] J.-Z. Tsai, J. Will, S. Hubbard-Van Stelle, H. Cao, S. Tungjitkusolmun, Y. B. Choy, D. Haemmerich, V. Vorperian, and J. Webster, "In-vivo measurement of swine myocardial resistivity," *Biomedical Engineering, IEEE Transactions on*, vol. 49, no. 5, pp. 472–483, 2002.

[78] D. Bouchaala, X. Chen, Q. Shi, O. Kanoun, and N. Derbel, "Comparative study of voltage controlled current sources for biompedance measurements," in *Systems, Signals and Devices (SSD), 2012 9th International Multi-Conference on*, March 2012, pp. 1–6.

[79] J. Meunier, N. Trayanova, and G. R.A., "Sinusoidal stimulation of myocardial tissue: effects on single cells," *J Cardiovasc Electrophysiol.*, vol. 10, no. 12, pp. 1619–1630, Dec. 1999.

[80] A. Pollard and R. Barr, "A new approach for resolution of complex tissue impedance spectra in hearts," *Biomedical Engineering, IEEE Transactions on*, vol. 60, no. 9, pp. 2494–2503, 2013.

[81] B. Gilbert, "Circuits for the precise synthesis of the sine function," *Electronics Letters*, vol. 13, no. 17, pp. 506–508, 1977.

[82] O. Ishizuka, Z. Tang, and H. Matsumoto, "Mos sine function generator using exponential-law technique," *Electronics Letters*, vol. 27, no. 21, pp. 1937–1939, 1991.

[83] M. Pessatti and C. dos Reis Filho, "Cmos analog sine function generator using lateral-pnp bipolar transistors," in *Devices, Circuits and Systems, 2002. Proceedings of the Fourth IEEE International Caracas Conference on*, 2002, pp. C030–C1–4.

[84] J. Fattaruso and R. Meyer, "Triangle-to-sine wave conversion with mos technology," *Solid-State Circuits, IEEE Journal of*, vol. 20, no. 2, pp. 623–631, Apr 1985.

[85] Z. Tang, O. Ishizuka, and H. Matsumoto, "Mos triangle-to-sine wave convertor based on subthreshold operation," *Electronics Letters*, vol. 26, no. 23, pp. 1983–1985, Nov 1990.

[86] T. J. C. Faes, H. V. der Meij, J. C. de Munck, and R. M. Heethaar, "The resistivity of human tissue (100 hz-10 mhz): a meta-analysis of review studies," *Physiol. Meas.*, vol. 20, no. 4, pp. R1–R10, 1999.

[87] Y.-G. Li, M. Haider, and Y. Massoud, "An efficient orthogonal pulse set generator for high-speed sub-ghz uwb communications," in *Circuits and Systems (ISCAS), 2014 IEEE International Symposium on*, June 2014, pp. 1913–1916.

[88] A. Nieuwoudt and Y. Massoud, "Analytical wide-band modeling of high frequency resistance in integrated spiral inductors," *Analog Int. Circ. and Sig. Proc.*, Feb. 2007.

[89] L. Zhang and Z. Zhou, "Research on orthogonal wavelet synthesized uwb waveform signal," in *Communications and Information Technology, 2005. ISCIT 2005. IEEE International Symposium on*, vol. 2, 2005, pp. 830–832.

[90] M. Ghavami, L. B. Michael, S. Haruyama, and R. Kohno, "A novel uwb pulse shape modulation system," *Wireless Personal Communications*, vol. 23, no. 1, pp. 105–120, 2002.

[91] L. Michael, M. Ghavami, and R. Kohno, "Multiple pulse generator for ultra-wideband communication using hermite polynomial based orthogonal pulses," in *Ultra Wideband Systems and Technologies, 2002. Digest of Papers. 2002 IEEE Conference on*, 2002, pp. 47–51.

[92] M. Ghavami, L. Michael, and R. Kohno, *Ultra Wideband Signals and Systems in Communication Engineering*, 2nd ed. Wiley, Feb. 2007.

[93] R. Dilmaghani, M. Ghavami, and A. Aghvami, "Uwb multiple-pulse generator and transmitter," in *Ultra Wideband Systems, 2004. Joint with Conference on Ultrawideband Systems and Technologies. Joint UWBST IWUWBS. 2004 International Workshop on*, 2004, pp. 117–121.

[94] B. Allen, S. Ghorashi, and M. Ghavarm, "A review of pulse design for impulse radio," in *Ultra Wideband Communications Technologies and System Design, 2004. IEE Seminar on*, 2004, pp. 93–97.

[95] A. Nieuwoudt, T. Ragheb, H. Nejati, and Y. Massoud, "Increasing manufacturing yield for wideband rf cmos lnas in the presence of process variations," *IEEE ISQED*, 2007.

[96] A. Nieuwoudt, T. Ragheb, and Y. Massoud, "Hierarchical optimization methodology for wideband low noise amplifiers," *IEEE ASP-DAC*, 2007.

[97] A. Nieuwoudt, T. Ragheb, H. Nejati, and Y. Massoud, "Numerical design optimization methodology for wideband and multi-band inductively degenerated cascode cmos low noise amplifiers," *IEEE TCAS I*, Jun. 2009.