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Growth And Analysis Of Transition-Metal-Doped Znse-Based Materials And Thin Film Structures For Mid-Infrared Optoelectronic Applications

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GROWTH AND ANALYSIS OF TRANSITION-METAL-DOPED ZNSE-BASED MATERIALS AND THIN FILM STRUCTURES FOR MID-INFRARED OPTOELECTRONIC APPLICATIONS

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PHYSICS

ABSTRACT

Transition metal (TM)-doped II-VI semiconductor thin films have been shown to be attractive materials for mid-infrared (mid-IR) laser sources due to broad applicability in the sensing and detection of a wide range of organic molecules. Specifically, when ZnSe is doped with Cr^{2+} ions, the resulting broadband emission characteristics in the 2-3 μm spectral range create the potential for tunable lasing in the mid-IR. This dissertation research is motivated by the need for low cost, efficient, portable materials to be incorporated into multilayered mid-IR optoelectronic devices providing appropriate optical confinement, efficient quantum confinement of carriers, and optical emission in the mid-IR spectral range.

The first primary objective of this dissertation research was to investigate the crystal quality of ZnSe-based thin film structures and the factors controlling the growth dynamics. This objective was pursued through X-ray Diffraction (XRD) analysis of numerous thin film structures, used to illuminate material properties associated with the crystalline quality and defect density of deposited layers. A significant focus was the pursuit of conditions for epitaxial growth of ZnSe-based materials by pulsed laser deposition (PLD). Conditions of epitaxy were researched in the growth of ZnS_xSe_{1-x} thin films to be used as lattice-matching layers in a multilayered structure deposited on cubic (100) GaAs substrates. Certain combinations of sulfur concentration and deposition

temperature were found to result in epitaxially-oriented films, but with dislocation densities on the order of ~10^{10} cm^{-2}. This was the first instance of growth of this material by PLD to our knowledge, and further progress was made in reducing dislocation densities with the addition of a Cr^{2+}:ZnSe layer at the GaAs interface. The effects of increasing thickness of the Cr^{2+}:ZnSe layer were studied in efforts to determine limits to epitaxy on this system. Epitaxially-oriented structures were achieved with the implementation of a Cr^{2+}:ZnSe layer (150 nm) at the GaAs interface, whereas polycrystalline structures were obtained at thicknesses above this critical value.

The second objective of this dissertation research was to explore the effects of crystallinity of thin film structures on the electrical properties of deposited ZnSe-based materials. This objective was pursued via electrochemical impedance spectroscopy (EIS) studies on various thin films structures for which the crystallographic properties were also determined. After annealing all samples in forming gas, impedance measurements were used to investigate electronic structure, and current-voltage measurements were utilized in extracting effective barrier heights in complex polycrystalline samples. A series of Cr^{2+}:ZnSe/$ZnS_{0.1}Se_{0.9}$ multilayered structures were deposited on GaAs substrates with deposition conditions known to produce polycrystalline films of $ZnS_{0.1}Se_{0.9}$ on GaAs in order to explore the resulting crystallographic and electrical properties as a function of thickness of the Cr^{2+}:ZnSe layer. Measured values for effective barrier heights of Schottky-like potential barriers contributed by the collection of grain boundaries throughout the samples showed an increase in effective barrier height with increasing thickness of the Cr^{2+}:ZnSe layer. This increase in effective barrier height also aligns with the relative increase of secondary diffraction peaks observed in the XRD glancing angle 2θ data, which

indicates an increase in the number of grain boundaries throughout the structures with increasing thickness. Measured values of specific contact resistance, indicative of the net resistance contributed from junction barriers primarily due to grain boundaries, were also observed to increase with thickness and polycrystalline features.

The third objective of this dissertation was the realization of a ZnSe-based electroluminescent device grown by PLD. This objective was achieved by growing a Cr^{2+}:ZnSe layer on top of conductive ITO/Glass substrates, utilizing a silicon mask to leave a portion of exposed ITO that would be used as the lower electrode. Ni contacts were deposited on the top surface of the ZnSe film, and electrical measurements were made utilizing a mesa geometry. Current densities as high as 30 mA/cm^2 were attained with an applied DC voltage of 16.7 V, and electroluminescence spectra were obtained for applied voltages with the range 10-20 V. The intensity of luminescence increased with increasing applied voltage, and the broad peak of emission was centered around ~650 nm. The broad nature of the peak suggests emission from multiple deep centers within ZnSe, and a side peak of low intensity at ~460 nm was observed and is likely the band-edge emission of ZnSe at room temperature. Absorption by chromium ions could partially contribute to the low measured intensities of emission in this 400-900 nm spectral region, and if due to sub-band excitation of chromium ions, would possibly result in emission in the mid-IR spectral range. An electroluminescent signal was also detected within the 2-3 μm spectral range with a similar experimental setup utilizing low and high pass optical filters. The intensity was too weak to obtain a spectrum of the detected luminescence, but this result is promising for future investigation of mid-IR emission from similar Cr^{2+}:ZnSe thin film structures.

DEDICATION

I dedicate this work to my beautiful and endlessly supportive wife, Ginger, as well as my children, Rowan and Joie, who make my life an enduring and beautiful adventure.

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First and foremost, I would like to express the deepest form of gratitude to my graduate mentor and friend, Dr. Renato P. Camata. He has been a valuable source of unwavering optimism, unmatched energy, and essential intellectual nourishment throughout the entirety of my graduate journey. I feel very fortunate and blessed to have had the opportunity to refine my skills as both a physicist and human being under his tutelage and guidance. He seems to never tire or lose his positive perspective, no matter the circumstances, and this is a trait I truly admire. I also want to extend this gratitude to the other members of my committee including Dr. Sergey B. Mirov, Dr. Mary Ellen Zvanut, Dr. David J. Hilton, Dr. Patrick Kung, and Dr. Sergey Vyazovkin for offering their time and knowledge to me throughout my graduate studies and research pursuits.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Transition metal (TM)-doped II-VI semiconductor thin films have been shown to be attractive materials for mid-infrared (mid-IR) laser sources [1]. These lasers have broad applicability in the sensing and detection of a wide range of organic molecules that pose biological and environmental threats, and these molecules exhibit unique absorption features in the spectral range 1-15 μm due to rotational and vibrational transitions [2]. When a II-VI semiconductor such as ZnSe is doped with TM ions such as Cr^{2+}, the resulting broadband emission characteristics in the 2-3 μm spectral range (due to emission from the dopant) create the potential for tunable lasing in the mid-IR. This research is motivated by the need for low cost, efficient, portable materials to be incorporated in mid-IR lasing and sensing devices for applications such as the detection of various organic molecules that exhibit absorption in the mid-IR such as atmospheric constituents, chemical and biological waste compounds, explosives, and toxic agents [3,4]. There are also potential applications in areas such as free space communication, climate pattern monitoring, medical diagnostics, and public health threat containment [5-7].

The fabrication of a multilayered device that provides appropriate optical confinement, efficient quantum confinement of carriers, and optical emission in the mid-IR spectral

range is highly desirable and could be integrated into numerous optical detection platforms utilizing optical nose and frequency comb chemical sensing approaches. Achieving such an efficient electrically-pumped laser source requires the integration of the mid-IR active layer (Cr^{2+}:ZnSe) with high-quality layers that allow for effective charge injection and confinement of the optical field for optical amplification.

1.2 Proposed Electroluminescent Structure for Mid-IR Lasing

Photoluminescence studies have demonstrated mid-IR emission under optical excitation in both bulk crystals and thin films structures of Cr^{2+}:ZnSe [8,9]. Achieving stimulated mid-IR emission of these structures via electrical excitation (electroluminescence) has proven to be much more challenging due to the values of high resistivity resulting from Cr^{2+}-doping of the ZnSe host crystal and compensation effects introduced in efforts to increase conductivity. Although unstable, electrically-pumped laser oscillation has been demonstrated via impact ionization in a waveguiding structure utilizing a similar TM:II-VI active layer (Cr^{2+}:ZnS) [10]. Since this result demonstrates mid-IR lasing due to impact ionization alone, the idea of integrating components providing charge injection and confinement of the optical field (via appropriate p-type and n-type conducting layers and waveguiding layers of appropriate index of refraction) is promising for realizing a mid-IR electroluminescent lasing device. Due to the need for a low-cost, electrically pumped, room temperature operated mid-IR laser with emission wavelength tunable over a wide range, a multilayered thin film structure providing charge injection, optical confinement of emission, and mid-IR emission of the active material would be ideal. Figure 1 illustrates the concept of a multilayered mid-IR electroluminescent structure. The ideal structure is

derived from a separate-confinement heterostructure configuration utilizing cladding and guiding layers based on the ZnMgSSe quaternary alloy system [11]. A $Zn_xMg_{1-x}S_xSe_{1-x}$ layer is lattice-matched to GaAs for x=0.1 and y=0.1, and is expected to have an index of refraction smaller than that of the active layer. Accordingly, this thin film would serve as a cladding layer for the structure, providing optical confinement. Appropriately-doped layers of ZnS_xSe_{1-x}, which is also lattice-matched to GaAs for x=0.06, would provide both injection of carriers and guiding of the radiation emitted in the active layer, shown in the figure as a 0.5−0.15 μm Cr^{2+}:ZnSe thin film to provide electroluminescence in the mid-IR.

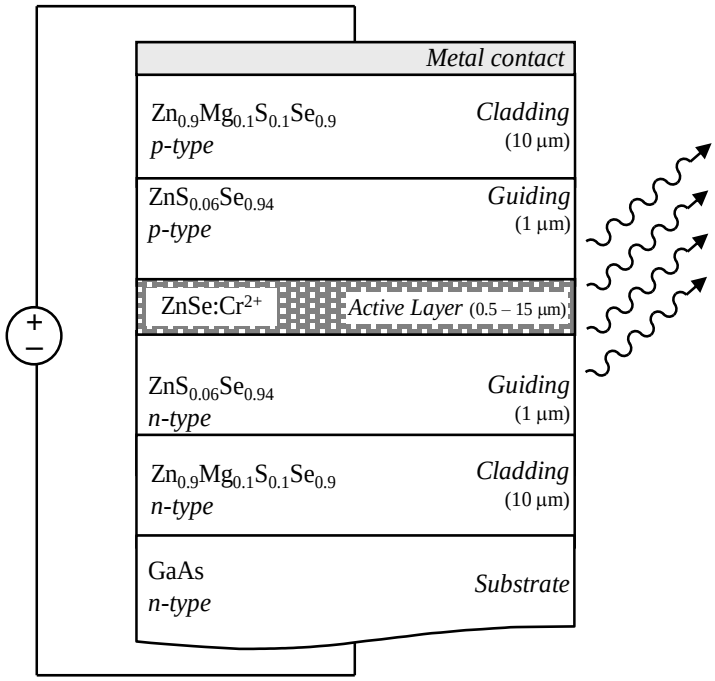


Figure 1. Concept of a multilayered thin film structure providing charge injection and optical confinement of mid-IR radiation emitted under electrical excitation (reproduced from [12] with permission © 2016 *MRS Proceedings*)

1.3 Dissertation Objectives

Considering the successful track record in recent literature of Cr^{2+}:ZnSe bulk crystals as mid-IR laser gain media under optical and electrical excitation, and the potential realization of a multilayered thin film structure for mid-IR electroluminescence (such as the structure concept illustrated in Figure 1), the focal point of this dissertation research is to investigate the basic materials and device physics processes that could enable a thin film mid-IR device operating under electrical excitation, namely:

(1) Elucidate the factors that control crystalline quality of material layers by pursuing epitaxial growth and reduction of defect densities in thin films grown by pulsed laser deposition (PLD) relevant to potential fabrication of a mid-IR electroluminescent device

(2) Investigate the effects of crystal quality of the mid-IR active layer (Cr^{2+}:ZnSe) of variable thickness on resulting electrical properties of ZnSe-based thin film structures

(3) Realize a PLD-deposited Cr^{2+}:ZnSe thin film structure displaying luminescence under electrical excitation

CHAPTER 2

PROPERTIES OF ZnSe-BASED MATERIALS

2.1 Transition Metal doped II-VI Materials

In order to achieve the desired mid-IR properties of the materials of interest for this research, transition metal (TM) dopants must be embedded into the host lattice. TM-doped II-VI compounds have been shown to be excellent candidates for laser material applications due to several factors. First of all, there are many chemically stable divalent TM dopant ions that enter the host matrix with little disturbance to the crystal structure and no need for charge compensation. Secondly, TM dopants tend to prefer tetrahedral coordination at the dopant site in II-VI crystals, which results in smaller crystal field splitting (relative to octahedral coordination sites) and pushes the dopant transitions deeper into the IR (see Fig. 2). Also, low phonon frequencies of heavy-ion host materials provide transparency over a wide spectral range, and decreases non-radiative relaxation rates [13].

TM:II-VI materials are also desirable candidates to provide broad tunability in the mid-IR due to strong electron-phonon coupling of the TM ions [14]. Properties such as low non-radiative decay and efficient transfer of energy from the host crystal to the TM ions also add to the promise of these materials as solid state, tunable laser materials in the mid-IR [15]. It is also interesting to note that TM impurities exhibit promising behavior in

environments that may exhibit quantum confinement effects, such as nanocrystals, quantum dots, and quantum wells. Nanocrystals of Mn doped ZnS studied by Bhargava et al [16] display shorter radiative lifetimes and higher quantum efficiencies than those seen in corresponding bulk samples. The oscillator strength of excitons bound to dopant centers in the thin film host is expected to be larger than that of a bulk crystal due to the higher electron-hole overlap factor and electron-hole exchange interaction term, both of which are increased by quantum confinement.

It has also been reported that near-bandgap luminescence quenching by the TM dopants was observed for ZnS quantum dots (2 nm) doped with Ni [17] which shows yet more promise for efficient energy transfer to the TM dopants. The Ni dopants introduce electron traps which resulted in non-radiative recombination and quenching of luminescence that increased with increasing Ni concentration, which is indicative that Ni is an effective trap for free carriers in the ZnS host. Previous studies on recombinative processes in CdTe quantum wells (QWs) show a large difference in decay time dependent on the presence of Cr ions [18]. It has been shown that the kinetic decay time of excitonic photoluminescence was significantly reduced with the addition of Cr ions to the QWs. These results show that many research directions in the use of II-VI semiconductor hosts with TM dopants remain unexplored. There is significant promise that efficient emission in the mid-IR with potential delivery of an electrically excited device is achievable in these systems.

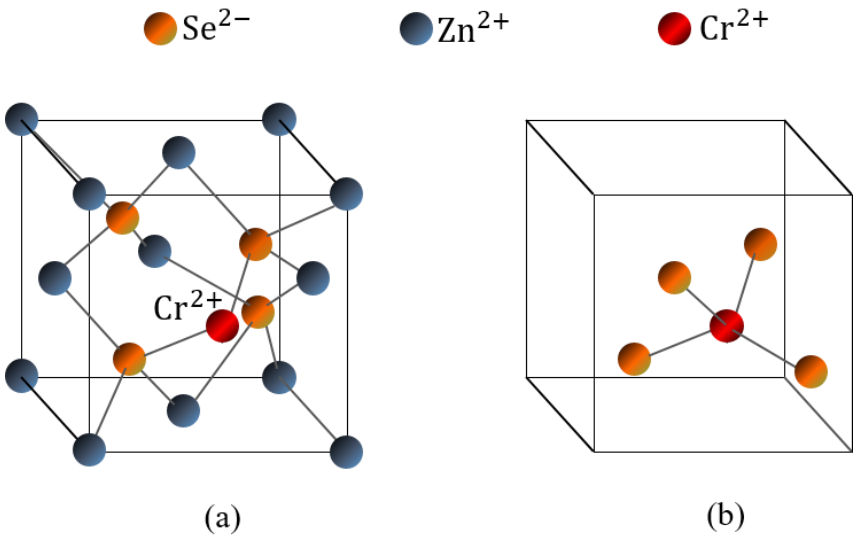


Figure 2. Illustration depicting (a) Cubic (Zinc-blende) Cr^{2+}:ZnSe crystal structure and (b) Tetrahedral coordination of Cr^{2+} at the Zn^{2+} site in ZnSe

2.2 Properties of Cr^{2+} in ZnSe Host

Among TM dopants in II-VI semiconductor host compounds, Cr is a standout dopant as there has been much study of its suitability for application in laser gain materials emitting in the mid-IR. When Cr enters the ZnSe lattice, it enters substitutionally at the Zn site, thus giving two electrons to the bonds and assumes its lattice-neutral charge state, Cr^{2+} [19]. As stated in the previous section, Cr takes on the tetrahedral coordination at the dopant site in ZnSe, which results in smaller crystal field splitting of the ^5D ground state than the more typical octahedral coordination. This tetrahedral coordination splits the ^5D ground state of the Cr^{2+} ion into a duplet excited state, ^5E, and a triplet ground state, ^5T, as shown in Figure 3. Notice the Stokes shift between absorption and emission bands is such that there is little self-absorption, which results in a broad emission window of approximately 2200-3000 nm [13].

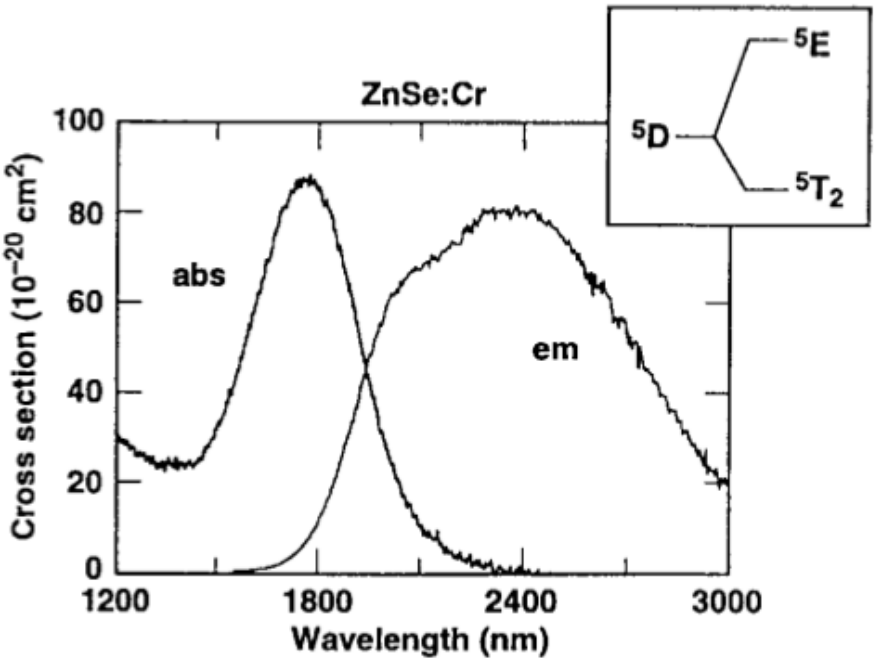


Figure 3. Absorption and Emission cross-sections of the ^5E to $^5T_2$ transition of Cr^{2+} in ZnSe (reproduced from [13] with permission © 1997 IEEE)

A primary challenge to utilizing Cr^{2+}:ZnSe for electroluminescence applications is achieving sufficient conductivity without significant compensation of the Cr^{2+} optical centers. Mid-IR electroluminescence of Cr^{2+}:ZnSe was achieved by Kim et al. [20] with n-conductivity provided by thermal diffusion of Al and Ag. However, the increased conductivity was accompanied by compensation of the Cr^{2+} centers, which resulted in relatively weak chromium electroluminescence. Further dopant studies have been conducted on the Cr^{2+}:ZnSe system via optical and electrical characterization of Cr^{2+}:ZnSe crystals with integration of Ag, Cu, Al, In, and Zn co-dopants to optimize mid-IR electroluminescence of the Cr^{2+} ions [21]. The best results were obtained with Ag:Cr:ZnSe samples of p-type conductivity featuring measured values of resistivity as low as 600 Ω•cm. Another recent study by the same group achieved co-doped Al:Cr:ZnSe samples with measured values of resistivity as low as 150 Ω•cm but displaying no mid-IR

electroluminescence [22]. However, these studies were performed using bulk semiconductor crystals rather than thin film structures. The subject of significant mid-IR electroluminescence from Cr^{2+}:ZnSe thin film structures remains largely unexplored and is a primary thrust of this research, considering the success achieved via photoluminescence and electroluminescence studies of Cr^{2+}:ZnSe bulk crystals.

2.3 Applications of ZnS_xSe_{1-x}

As the respective lattice parameters of ZnSe and ZnS are 5.6686 Å and 5.4093 Å [23], the integration of sulfur into the ZnSe lattice by mixing ZnS and ZnSe powders to produce the ternary alloy ZnS_xSe_{1-x} widens the band gap (see Figure 4), which increases the blue response of devices [24], and has several optical applications including tunable UV photo detectors, visible laser diodes and light emitting diodes [25]. However, the primary incentive to the integration of S into the ZnSe lattice is to lattice match the resulting ZnS_xSe_{1-x} film to the (100) GaAs substrate (5.6535 Å [26]) to encourage epitaxial growth of optical quality layers.

Epitaxial growth of each layer is desired to achieve the electronic and optical properties necessary for successful integration into a multilayered lasing device (see Figure 1) [11, 27]. A similar configuration has been very successful in the demonstration of low threshold current blue-green lasers based on II-VI materials [28, 29]. Due to the lack of commercially available MgSe and MgS powders of high purity at the time of this research, this dissertation does not address growth and characterization of the proposed quaternary cladding layers, but focuses more heavily on the ternary guiding layer material. ZnS_xSe_{1-x}

has been shown to be an effective waveguiding material in ZnSe/GaAs systems when grown via molecular beam epitaxy [30], but never before has this material been reported to be successfully grown by means of PLD prior to this study.

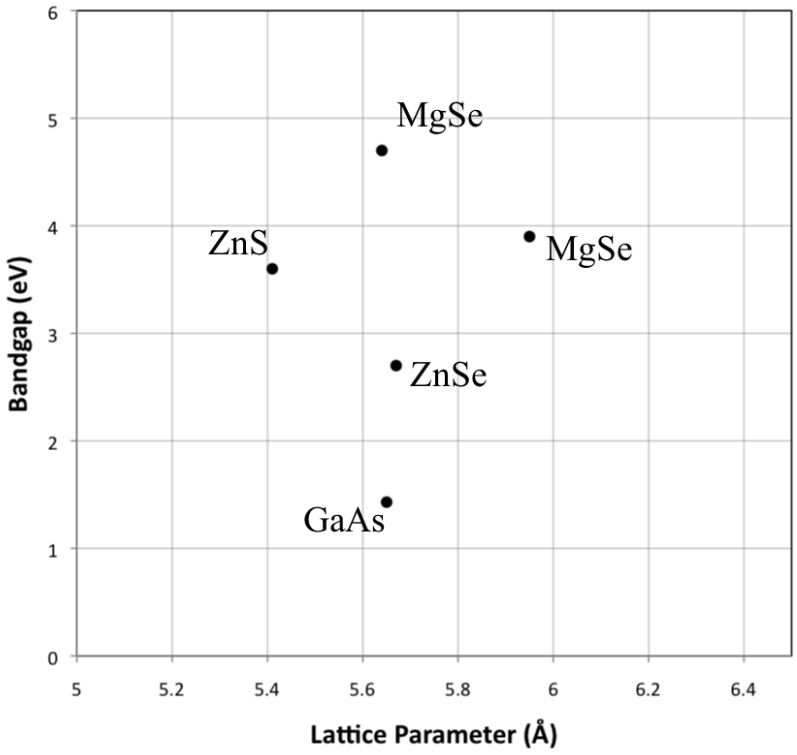


Figure 4. Plot showing Bandgap (eV) vs Lattice Constant (Å) for various compound semiconductors, including ZnSe and ZnS

CHAPTER 3

GROWTH METHODS FOR ZnSe-BASED THIN FILM STRUCTURES

3.1 Pulsed Laser Deposition Method

All semiconductor thin films for this research were grown by the pulsed laser deposition (PLD) method, which is a form of physical vapor deposition where the beam of a high power pulsed laser source is transmitted into a vacuum chamber where it is focused onto an ablation target of desired elemental composition. Upon incidence of the beam, the target material is instantaneously melted and vaporized, emitting ablated species from the surface to form a plasma plume that rapidly cools and expands towards the substrate, where the species ultimately condenses to form a thin film.

A key advantage to using PLD as a growth method is the preservation of the stoichiometry of the ablation target to the resulting deposited films [31,32]. The PLD experimental setup consists of a stainless steel vacuum chamber that is pumped down by means of a turbomolecular pump capable of achieving base pressures on the order of 10^{-8} Torr during thin film deposition. Substrates are mounted onto a machined Ni plate that is loaded onto a heating coil inside the deposition chamber. In-house prepared ablation targets of desired material composition can be loaded onto a rotating target carousel that can hold up to six targets at one time, making it possible to potentially deposit *in situ* multilayered thin film heterostructures composed of up to six different materials. Once the substrate and

target(s) have been loaded into the chamber and pumped down to the desired base pressure, a KrF excimer UV laser emitting at 248 nm with a pulse duration of 30 ns can be passed through one of the chamber's quartz windows and focused through an optical system to achieve a laser spot size of desired area incident on the ablation target. During deposition the substrate and ablation target can be rotated, and the substrate can be heated and maintained at temperatures approaching 1000°C throughout the deposition process.

PLD is an extremely versatile growth method that allows for relatively fast rates of film growth and is capable of performing thin film depositions using many different atomic and molecular constituents. This is in stark contrast with methods such as molecular beam epitaxy (MBE), which often requires an entire system to be devoted to film growth of a primary molecular species to avoid cross-contamination of deposited samples. Both the versatility and relatively quick growth process of PLD make it an effective method for growing novel thin film materials with various elemental compositions and potential dopants, as well as growing *in situ* multilayered thin film structures of desired layer composition.

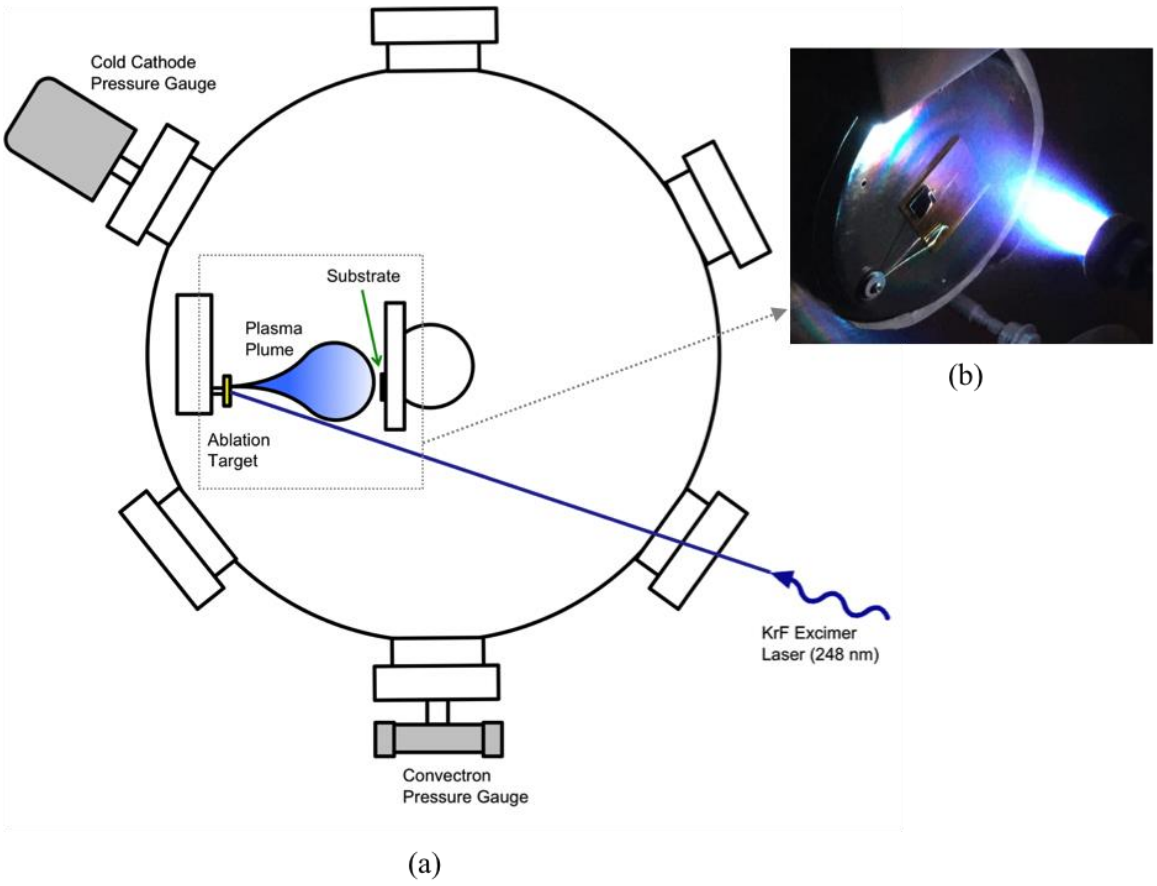


Figure 5. (a) Schematic illustrating basic layout of Pulsed Laser Deposition system and (b) actual image of PLD plume during deposition of ZnSe on masked ITO substrate

3.2 Ablation Target Production

As stated in the previous section, a key advantage of thin film synthesis by PLD is the overall preservation of composition and stoichiometry from the ablation target to the deposited film. That being said, each ablation target used in this research was made in-house from high purity powders of the constituent species. In general, the appropriate powders were weighed to achieve the correct stoichiometry, then mechanically mixed via mortar and pestle before being compacted at room temperature in a stainless steel cast and die at ~5000 PSI for ~10 minutes using a hydraulic press (see Figure 6). In efforts to avoid

the occurrence of undesired reactions during annealing, the compressed pellet was then removed and placed inside of a quartz ampoule and pumped down to ~10 mTorr via a turbo-molecular pump before sealing the ampoule with an oxyhydrogen torch. The sealed ampoule was then placed into a furnace to anneal at 950°C for 3 days to prevent the target from pulverization upon ablation by the excimer laser during deposition. After annealing, the compressed pellet now resembles a solid ceramic disk that can now be mounted into the PLD chamber for ablation.

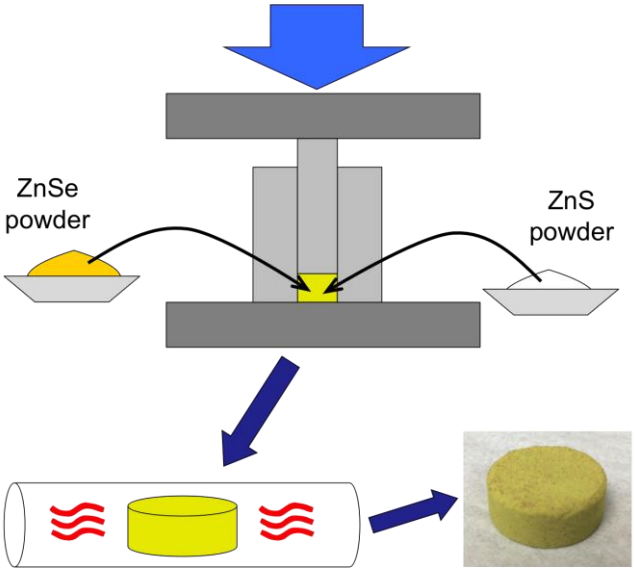


Figure 6. Schematic showing overview of ablation target production process for pulsed laser deposition

3.3 Thin Film Deposition

A major motivating factor to thin film deposition by PLD is the capability to vary an array of different deposition parameters that directly affect the properties of the resulting film. Examples of parameters that can be easily varied and selected for a given thin film deposition include base pressure of the chamber, laser energy, pulse count, repetition rate, laser spot size, substrate temperature, substrate orientation, rate of substrate rotation, and

elemental composition of ablation target (among others). Film thickness can be selected by varying the laser energy, laser spot size, repetition rate, and pulse count, all of which can be computer controlled from a single user interface. Considering the significant role that parameters such as growth temperature, laser energy density, and pulse count (among others) can play in determining the crystal structure, phase, defect density, and thickness of the resulting films, PLD provides many valuable degrees of freedom to control the characteristics of the deposited thin films produced with the system. For this research, PLD was used to produce an assortment of different materials and structures that were subsequently analyzed using several characterization techniques to extract optical, electrical, and/or crystallographic properties.

3.4 Metallic Contact Deposition

In order to make meaningful electrical measurements, high quality, intimate metallic contacts must be deposited onto each sample. The optimization of the contact deposition process plays a significant role in device performance and characterization, as surface defects at the metal-semiconductor interface can skew measurements, trap electrons, and even cause device failure. Before attempting to deposit contacts onto the various ZnSe-based films deposited via PLD for this research, contacts were deposited on well-characterized, single crystal semiconductor samples (n-type Si) as an attempt to show the efficacy of the Capacitance-Voltage (C-V) method in determining the dopant concentration of a given sample. The electrical properties of the Si wafers were known within a narrow range of uncertainty and were therefore useful as an experimental standard to verify that

our characterization approach yielded reliable dopant concentration values. A variety of deposition methods and contact materials were used to investigate their effects on the characterization process. The different methods tested with our first approach include pulsed-laser deposited Cu contacts and contacts applied via Ag paint using several application methods. After analyzing the samples via electrochemical impedance spectroscopy to determine resistivity and dopant concentration of the Si wafer, it was found that all samples for which metallic contacts were deposited and dopant concentrations measured via the C-V method yielded measurements that fell within the accepted range of resistivity values provided by the manufacturer (see Figure 8). This exercise (documented in section 4.5) demonstrates our ability to measure, with confidence, the dopant concentration of subsequent doped semiconductor samples fabricated for this research, provided each sample fits the specific criteria and assumptions made under the abrupt approximation.

Following this preliminary study on metallic contact fabrication, a Magnetron Sputtering deposition system was designed and fabricated in-house for deposition of metallic contacts with the capability to deposit contacts using a wide variety of materials and geometries in a timely and efficient manner. The majority of metallic contacts deposited onto thin film samples produced for this research that required electrical measurements were deposited using the Magnetron Sputtering deposition system.

CHAPTER 4

ELECTRICAL CHARACTERIZATION METHODS FOR ZnSe-BASED THIN FILM STRUCTURES

4.1 Electrochemical Impedance Spectroscopy

Electrochemical Impedance Spectroscopy is a measurement technique in which an electrical stimulus (voltage or current) is applied to a sample, and the electrical responses of the sample are observed and studied. Perhaps the most distinctive feature of this technique is the application of an AC signal of small amplitude that can be applied at various frequencies (depending on the mechanism or structure of interest being measured), which illuminates the spectroscopic nature of this characterization technique. The system's response to applied AC signals of various frequencies gives information about the electronic structure, interfaces, and possible reactions occurring within the sample [33]. Access to such information which provides distinction between characteristics of interfaces present in thin film structures and bulk semiconductor layers makes this a valuable technique for pursuing dissertation objective (2).

The impedance of a material is given by

$$Z(\omega) = Z' + iZ'' = R - i\frac{1}{\omega C} \qquad (1)$$

where Z *'* and Z *''* represent the respective real and imaginary components of the impedance, where $Z' = R$ and $Z'' = -\frac{1}{\omega C}$, and the modulus of $Z(\omega)$ is given by

$$|Z(\omega)| = \sqrt{(Z')^2 + (Z'')^2} = \sqrt{R^2 + (1/\omega C)^2} \qquad (2)$$

A useful way of visualizing impedance data for analyzing electrical properties of complex structures is via the Nyquist plot, which displays Z" versus Z' as a function of the applied DC bias and the frequency of the applied AC signal. Depending on the electrical properties of the sample, conclusions about corresponding equivalent circuit models may be obtained from the Nyquist plot. From equation 1, it is transparent that the real and imaginary components of the impedance will vary with the resistance and capacitance of the sample, and the frequency response dictates where these features arise on the Nyquist plot. For example, a purely capacitive sample will yield a vertical line on the Nyquist plot, and a resistance added in series would shift this vertical line in the +x direction with increasing magnitude of the series resistance (see Figure 7a). If the electronic structure of the sample has both a capacitive and resistive element acting in parallel, the resulting Nyquist plot will resemble a semicircle with a diameter representative of the magnitude of the resistance (see Figure 7b), and the frequency at the semicircle maximum is equal to the characteristic frequency of the equivalent circuit, given by

$$\omega_C = \frac{1}{\tau} = \frac{1}{RC} \qquad (3)$$

The characteristic frequencies of many samples in this research were used to determine the source of the mechanism being probed in the measurement, whether it be due to a thin film layer, interface, grain boundary, etc. This feature alone proved valuable throughout this dissertation research to characterize and provide information for several samples.

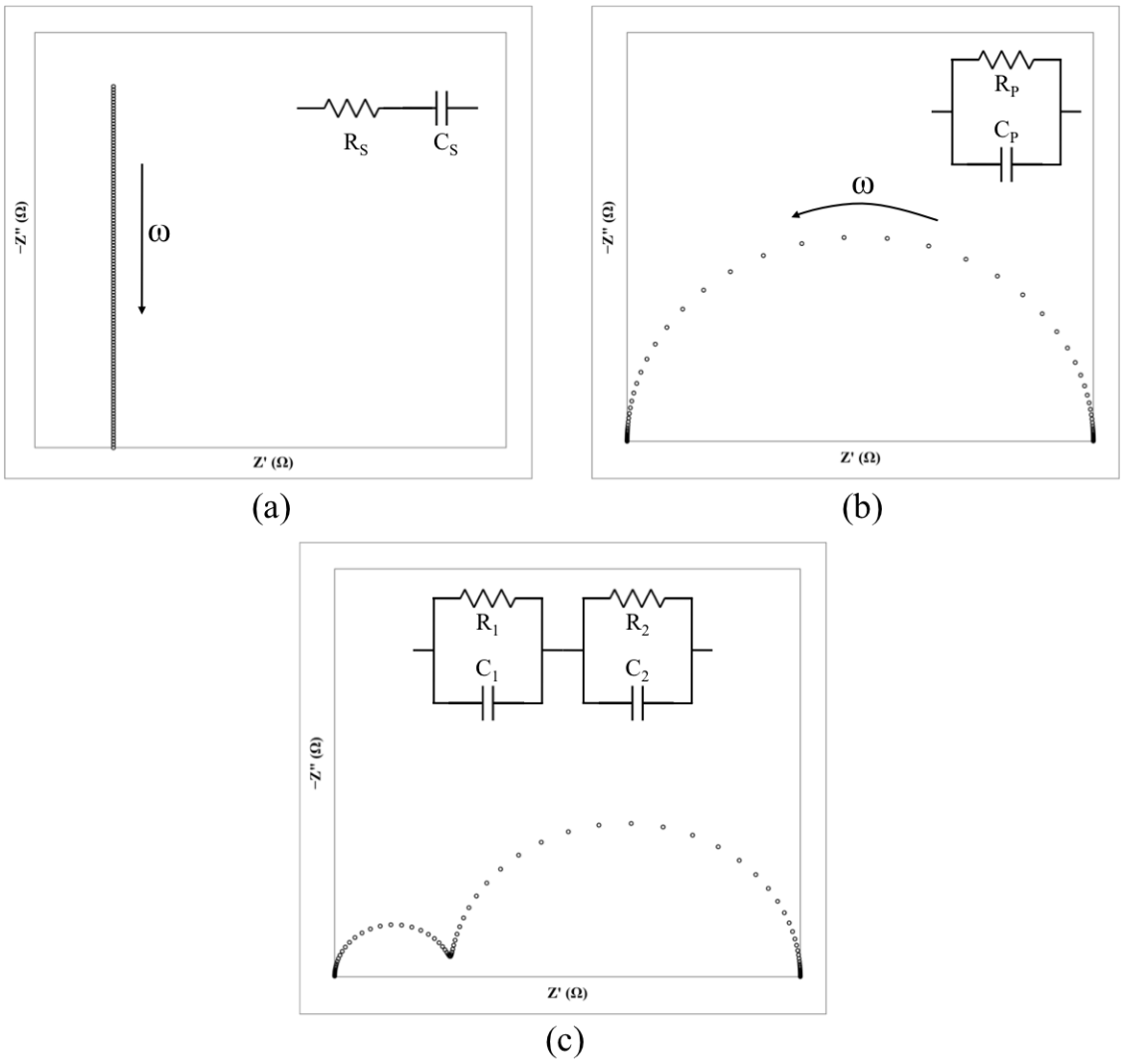


Figure 7. Basic Circuit Models with associated Nyquist Impedance plots including the following combinations: (a) resistor and capacitor in series, (b) resistor and capacitor in parallel, and (c) combination of parallel RC circuits wired in series

Without using the characteristic capacitance obtained from the Nyquist plot, the mechanism or structure being probed in the measurement would lack specificity. As seen in Figure 7c, multiple arcs may arise when looking at more complicated structures, which is the case for many of the samples fabricated throughout this dissertation research. Since the vast majority of the films grown for this research consisted of semiconductor materials with both resistive and capacitive elements, there were many opportunities for which EIS

measurements provided informative insight into metal/semiconductor interfaces, various material properties, and behaviors of different components of thin film structures with variable frequency and applied DC bias voltage.

4.2 Interfacial Junctions

Deposition of multilayered thin film structures inevitably introduces material interfaces, which can lend significant physical contributions to the energy band structure, charge transport properties, and preferred crystallographic orientation of the resulting structures. For the studies conducted in this dissertation, both the p-n junction and metal/semiconductor junction possess relevant physics to several structures of interest and will be individually investigated. As one of the cornerstones of semiconductor physics, p-n junction theory is an appropriate starting point for this topic.

Within a p-n junction, there are two primary limiting cases for approximating dopant profiles: the abrupt junction and the linearly graded junction (see Figure 8). The abrupt junction model has been used throughout this dissertation since this approach most accurately describes the interfaces within thin film structures fabricated for this research. For example, the abrupt approximation adequately describes alloyed junctions, shallowly diffused junctions, and ion-implanted junctions as opposed to deeply diffused junctions for which the linearly graded approximation is more fit [35]. Due to the much larger electron concentration on the n-side relative to the p-side and similar imbalance with

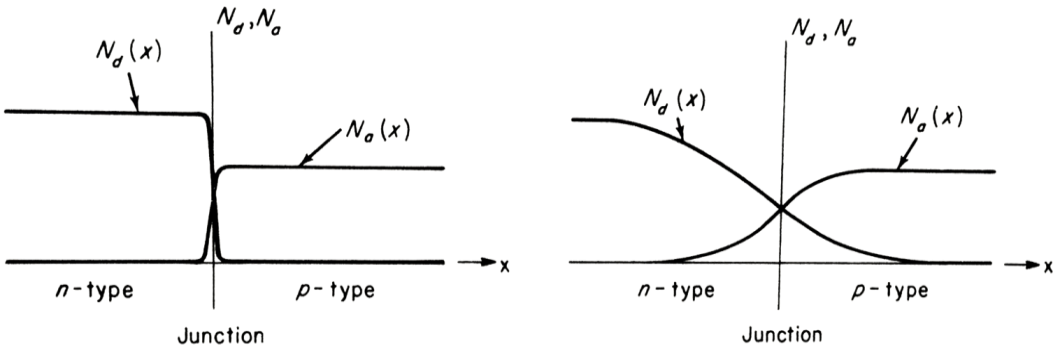


Figure 8. Net concentrations of donor impurities (N_d) and acceptor impurities (N_a) in the neighborhood of an (a) abrupt p-n junction and (b) a linearly graded p-n junction (reproduced from [34] with permission)

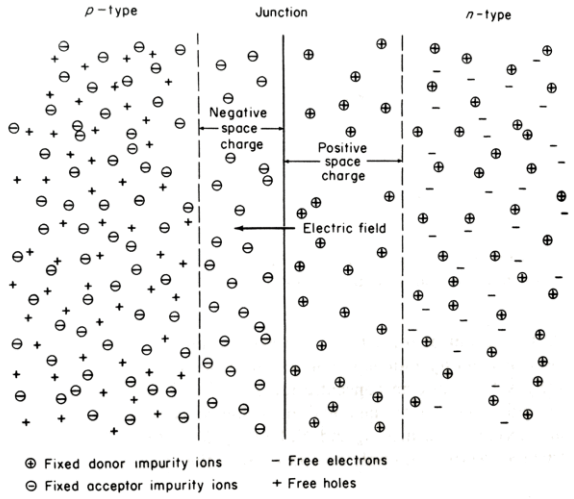


Figure 9. Diagram showing formation of carrier-depleted space charge regions and internal electric field initiated by diffusion of carriers near abrupt p-n junction (reproduced from [34] with permission)

respect the concentration of holes on the p-side relative to the n-side, there is a significant gradient in electron and hole concentrations at the interface between the two regions upon junction formation. These large concentration gradients initiate diffusion currents, where electrons from the n-side and holes from the p-side flow to the side of opposite majority type, which depletes the regions near the junction of majority carriers (see Figure 9). As the regions become depleted of majority carriers, the acceptor and donor ions left behind

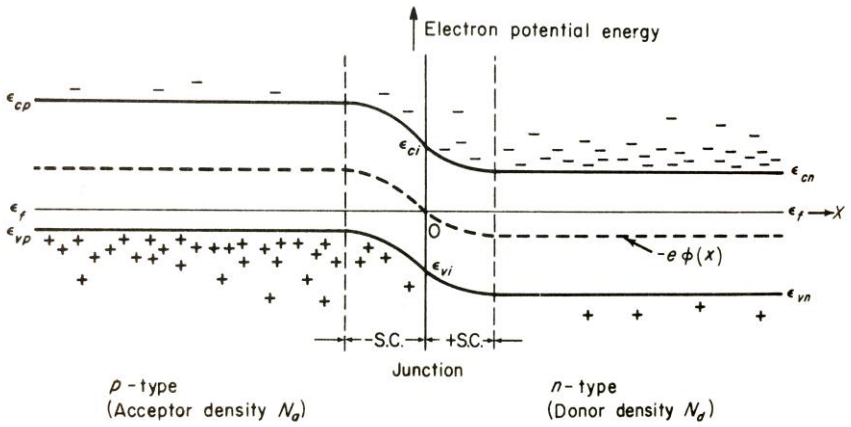


Figure 10. Diagram showing energy band configuration in the neighborhood of a p-n junction with no applied bias voltage (reproduced from [34] with permission)

create a "built-in" electric field across the junction. The direction of the field is oriented to oppose the outward flow of electrons from the n-region as well as the outward flow of holes from the p-region. These regions near the junction that are depleted of majority carriers are known as space charge regions, and the configuration of the positive and negative space charge resembles an electric dipole layer with a difference in potential between the region edges known as the internal contact potential (ϕ_0). This notion of two space charge layers containing equal and opposite amounts of charge is reminiscent of a parallel plate capacitor, and the resulting capacitance as a function of externally applied bias voltage will be expanded upon later in this chapter.

Figure 10 shows a diagram of the potential energy as a function of position in the neighborhood of the junction where the existence of the built-in electric field is depicted via the curvature of the potential bands across the space charge regions. The internal contact potential is represented by the difference between conduction band (or valence band) heights in the n- and p-regions (beyond the space charge regions), and a potential barrier impeding electron flow from the n-region to the p-region (and vice-versa for

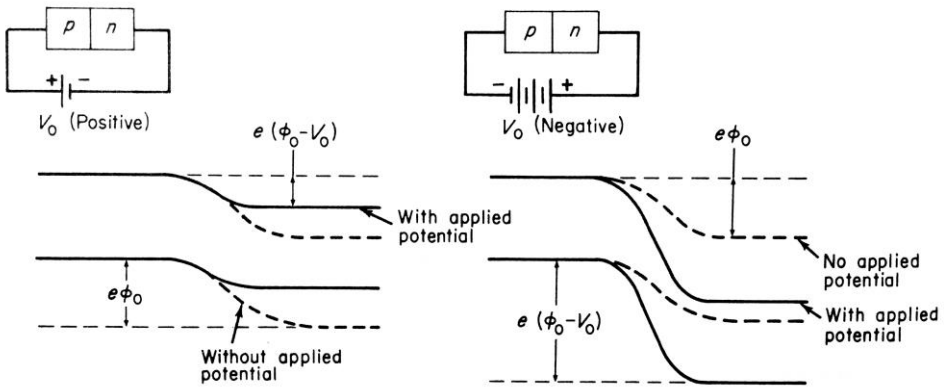


Figure 11. Energy band diagrams showing (a) forward bias and (b) reverse bias voltage effects on a p-n junction (reproduced from [34] with permission)

holes) is created at the interface. Notice the uniformity of the Fermi level (ε_f) throughout the entire structure, indicating thermal equilibrium and no applied bias voltage. When an external voltage is applied across a sample with a p-n junction, most of the voltage drop occurs across the carrier-depleted space charge regions due to the higher resistivity of these regions relative to the surrounding crystal [34]. This detail is significant as it suggests that any other voltage drops occurring outside of the space charge regions to be negligible in comparison to the voltage drop across the junction (in most practical cases).

In general, there are two distinct charge transport regimes achieved determined by the polarity of the applied bias voltage (see Figure 11). When an external voltage is applied with the positive terminal connected to the p-region, the effective barrier height is decreased for electrons flowing from the n-region into the p-region (and for holes flowing from the p-region into the n-region) and is known as the forward bias state. The reverse bias state is achieved with the opposite polarity of the externally applied bias voltage (negative terminal connected to p-region), which increases the effective barrier height with increasing magnitude of the bias voltage. In the reverse bias state, the carrier-depleted region increases in width with increasing bias. As a result, the capacitance of this region

(known as the depletion capacitance) decreases with increasing bias in accordance to the standard equation for capacitance per unit area, given by

$$C = \frac{\varepsilon_s}{d} = \frac{\varepsilon_s}{W_D} \tag{4}$$

where ε_s is the semiconductor permitivitty and W_D is the width of the depletion region. A similar effect is observed in metal/semiconductor junctions, which can result in the same type of rectified current flow and differential capacitance, and can be used to calculate material and junction parameters of interest. Similar to p-n junction formation, when a metal and semiconductor are brought into intimate contact, a potential barrier is formed at the interface due tot the fact that the Fermi levels in both materials must coincide at thermal equilibrium. For each material, the work function represents the energy difference between the respective Fermi levels and the vacuum level (see Figure 12).

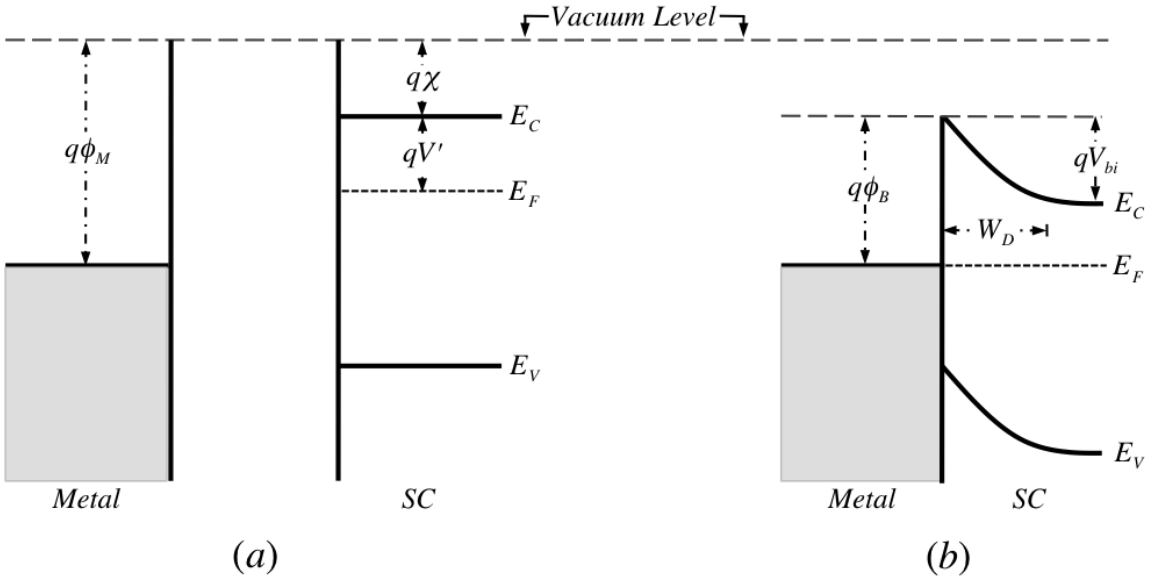


Figure 12. Schematic of Energy Band Diagrams (a) before and (b) after ideal junction formation between metal and n-type semiconductor

Assuming an ideal metal/semiconductor junction (no surface states present at the interface), the Fermi level in the semiconductor must decrease by a value equal to the difference in the work functions of the metal and semiconductor. The work function of the semiconductor is given by the sum of the electron affinity and the energy difference between the bottom of the conduction band and the Fermi level of the semiconductor:

$$q\phi_{SC} = q\chi + qV' \tag{5}$$

where

$$V' = E_C - E_F \tag{6}$$

In order to cause the Fermi level in an n-type semiconductor (with $\phi_M < \phi_{SC}$) to coincide with the Fermi level of the metal, electrons must flow out of the semiconductor and into the metal, thereby lowering the Fermi level in the semiconductor. This region of the semiconductor that has been depleted of electrons is called the depletion region, and a layer of negative charge builds up at the metal/semiconductor interface. The ionized donors left behind in the semiconductor represent a region of positive charge, which just as in the p-n junction, is known as the positive space charge region. The potential difference established in this process creates an electric field that extends into the semiconductor bulk. Since the magnitude of the electric field is maximum at the interface, an electron at rest at the bottom of the conduction band in the interior of the semiconductor will have a different potential energy than a similar electron at the metal/semiconductor surface. As a result, the conduction band (and valence band) edges are shifted with respect to the Fermi level, causing the curvature of the energy bands seen in Figure 12b.

The potential barrier created by this process of joining the two materials plays a pivotal role in the current-rectifying behavior of the junction, which will be investigated in

a later section. However, more immediate attention will be given to the equations that dictate the potential profile of the energy bands for a given junction. Perhaps the most important equation for semiconductor device operation is Poisson's equation, which relates the second derivative of the potential (with respect to position) to the charge distribution throughout the semiconductor. In the general case, Poisson's equation in one-dimension is given by

$$-\frac{\partial^2 \phi}{\partial x^2} = \frac{\rho(x)}{\varepsilon_S} \tag{7}$$

where the general expression for the charge distribution is given by

$$\rho(x) = q\left[p(x) - n(x) + N_D(x) - N_A(x)\right] \tag{8}$$

The electron and hole concentrations as a function of position can be expressed as

$$n(x) = U_C e^{-(\varepsilon_c(x) - \varepsilon_{fn})/kT} \tag{9}$$

$$p(x) = U_V e^{-(\varepsilon_{fp} - \varepsilon_v(x))/kT} \tag{10}$$

where ε_{fn} and ε_{fp} represent the Fermi level on the n-side and p-side of the junction, respectively. Also, $\varepsilon_c(x)$ and $\varepsilon_v(x)$ represent the position-dependent conduction and valence band edges, respectively, and are related to the potential function $\phi(x)$ by

$$\varepsilon_c(x) = -q\phi(x) + \varepsilon_{ci} \tag{11}$$

$$\varepsilon_v(x) = -q\phi(x) + \varepsilon_{vi} \tag{12}$$

where ε_{ci} and ε_{vi} represent the intrinsic energy values of the conduction band and valence band edges. Substituting these values into equation 8 yields the following expression for the charge distribution:

$$\rho(x) = q\left[U_V e^{-(\varepsilon_{fp} - \varepsilon_{vi} + q\phi(x))/kT} - U_C e^{-(\varepsilon_{ci} - \varepsilon_{fn} - q\phi(x))/kT} + N_D(x) - N_A(x)\right] \tag{13}$$

Substituting the charge distribution in equation 16 into Poisson's equation gives

$$-\frac{\partial^2\phi}{\partial x^2}=\frac{q}{\varepsilon_S}\left[U_V e^{-(\varepsilon_{fp}-\varepsilon_{vi}+q\phi(x))/kT}-U_C e^{-(\varepsilon_{ci}-\varepsilon_{fn}-q\phi(x))/kT}+N_D(x)-N_A(x)\right] \quad (14)$$

The general solution of equation 14 is non-trivial, but in the case of thermal equilibrium and no applied bias voltage, the Fermi levels on both sides of the junction must be equal:

$$\varepsilon_{fn}=\varepsilon_{fp}=\varepsilon_f \quad (15)$$

which enables the following substitution for the intrinsic carrier concentration, n_i :

$$U_V e^{-(\varepsilon_f-\varepsilon_{vi})/kT}=U_C e^{-(\varepsilon_{ci}-\varepsilon_f)/kT}=n_i \quad (16)$$

Rewriting Poisson's equation again using the substitution from equation 16 gives

$$-\frac{\partial^2\phi}{\partial x^2}=\frac{q}{\varepsilon_S}\left[n_i e^{q\phi(x)/kT}-n_i e^{-q\phi(x)/kT}+N_D(x)-N_A(x)\right] \quad (17)$$

Rearranging terms and using the definition of the hyperbolic sine function gives

$$-\frac{\partial^2\phi}{\partial x^2}=\frac{qn_i}{\varepsilon_S}\left[2\sinh\left(\frac{q\phi(x)}{kT}\right)+\frac{N_D(x)-N_A(x)}{n_i}\right] \quad (18)$$

With the appropriate assumptions, Equation 18 is valid for both p-n junctions and metal/semiconductor junctions under thermal equilibrium conditions, and can be solved using the appropriate boundary conditions.

4.3 Determination of Barrier Height

The potential barrier created when joining a metal and semiconductor plays a significant role in the electrical transport properties of the junction. Determination of junction properties, such as the height of the potential barrier or dominant mechanisms of charge transport across such junctions, is pivotal in fulfilling dissertation objections (2) and (3) due to the relevance of interfacial junctions to the investigation and separation of

resistances associated with interfaces within thin film structures studied in this research. For such a metal/semiconductor junction, the barrier height is ideally the difference in the work function of the metal and the electron affinity of the semiconductor and is given by

$$\phi_B = q\phi_M - q\chi \tag{19}$$

but can vary from equation 4 due to charge states present at the interface. The primary method utilized in this research for characterization of barrier height involves current density as a function of applied voltage. Assuming the charge transport process is dominated by thermionic emission, the relationship between current density *J* as a function of applied voltage *V* is given by [36]

$$J = J_S\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{20}$$

where J_S is the saturation current density given by

$$J_S = A^{**}T^2\exp\left(\frac{-q\phi_B}{kT}\right) \tag{21}$$

and n is the ideality factor, which is defined as

$$n = \frac{q}{kT}\frac{\partial V}{\partial(\ln J)} \tag{22}$$

and A^{**} is the effective Richardson constant for thermionic emission, which is given by

$$A^{**} = \frac{4\pi q m^* k^2}{h^3} \tag{23}$$

where m^* is the effective electron mass in the semiconductor. For values of V>>kT/q, equation 20 can be approximated to be

$$J \approx J_S\exp\left(\frac{qV}{nkT}\right) \tag{24}$$

Taking the natural log of both sides of equation 24 and rearranging terms yields

$$\ln J = \frac{qV}{nkT} + \ln J_S \tag{25}$$

By plotting the natural log of the current density as a function of applied voltage, the barrier height of the junction can be obtained by extrapolating a linear fit to the log-linear region to determine the y-intercept. Setting the value of the y-intercept equal to $\ln(J_S)$ and plugging in appropriate values for the effective Richardson constant (A^{**}) and temperature (T) allows for a straightforward determination of the barrier height of the junction. Applications of this method will be expanded upon further in Chapter 6.

4.4 Capacitance-Voltage Method

In order to discern between characteristics of material junctions and thin film layers, which is essential in assigning associated resistances to their respective sources as is required for fulfilling dissertation objectives (2) and (3), the capacitance-voltage method can reveal information about the individual components in a multilayered structure by observing the capacitive properties of a given sample with variable applied voltage. This method can be utilized to calculate dopant concentrations in semiconductor thin film samples, which is an effective method for observing properties of a charge carrier injection structure. The capacitance-voltage method utilizes a solution to Poisson's equation obtained under the abrupt approximation to establish a relationship between applied voltage and variable capacitance of material junctions between n-type and p-type semiconductors or between a metal and semiconductor. Since the majority of the work done in this research using this method has been applied to metal/semiconductor interfaces, the corresponding theory will be immediately explored for an interface between a metal and an n-type semiconductor. Applying the abrupt approximation to the general form of Poisson's equation (equation 7)

essentially assumes the charge distribution to be non-zero only within the depletion region, and approximates the charge distribution within the region to be dominated by donor dopants:

$$\rho(x) \approx qN_D \quad for \quad 0 < x \le W_D \tag{26}$$

$$\rho(x) \approx 0 \quad for \quad x > W_D \tag{27}$$

Substituting this approximation for the charge distribution in equation 7 gives

$$-\frac{\partial^2 \phi}{\partial x^2} \approx \frac{qN_D}{\varepsilon_S} \quad for \quad 0 < x \le W_D \tag{28}$$

The relationship between electric potential and electric field is given by

$$-\frac{\partial \phi}{\partial x} = E(x) \tag{29}$$

Therefore, equation 28 can be rewritten as

$$-\frac{\partial^2 \phi}{\partial x^2} = \frac{\partial E}{\partial x} = \frac{qN_D}{\varepsilon_S} \quad for \quad 0 < x \le W_D \tag{30}$$

By integrating equation 30 and applying the boundary condition that E=0 when $x=W_D$, an expression for the electric field is obtained to be

$$E(x) = \frac{qN_D}{\varepsilon_S}(W_D - x) \tag{31}$$

From an energy band perspective, the slope of the potential profile should display maximum deviation at the interface (x=0) from the flat bands in the semiconductor bulk, and the magnitude of this maximum electric field is given by

$$E_{\max} = \frac{qN_D W_D}{\varepsilon_S} \tag{32}$$

Integrating equation 31 and applying the boundary condition $\phi=0$ when $x=W_D$ yields the potential distribution as a function of position

$$\phi(x) = \frac{qN_D}{\varepsilon_S}\left(W_D x - \frac{x^2}{2} - \frac{W_D^2}{2}\right) = \frac{qN_D}{\varepsilon_S}\left(W_D x - \frac{x^2}{2}\right) - V_{bi} \qquad (33)$$

Since ϕ=0 was chosen to occur at the conduction band edge deep in the semiconductor bulk, the maximum value of the potential profile is achieved at the interface (x=0) and is equal in magnitude to that of the built-in potential. The minus sign in front of the built-in potential term in equation 33 is dealt with once the electron charge is substituted for *q*. To solve for the magnitude of the depletion width at equilibrium, W_D can be solved for in equation 36 at the edge of the depletion region ($x=W_D$):

$$W_D = \sqrt{\frac{2\varepsilon_S}{qN_D} V_{bi}} \qquad (34)$$

To obtain a more accurate result, a correction factor of kT/q must be introduced to decrease the width of the depletion region due to the presence of the majority carrier distribution tail at the boundary of the region [35]:

$$W_D = \sqrt{\frac{2\varepsilon_S}{qN_D}\left(V_{bi} - kT/q\right)} \qquad (35)$$

In the case of a p-n junction, there would be a distribution tail for electrons in the n-region and holes in the p-region, so this correction factor doubles in magnitude. As previously described, the depletion region behaves as a dielectric, and the space charge layers containing equal and opposite amounts of charge complete the picture of a parallel plate capacitor. When a non-zero bias voltage is applied to the junction, the Fermi levels in the metal and semiconductor no longer coincide, and the band edges shift within the semiconductor relative to the metal.

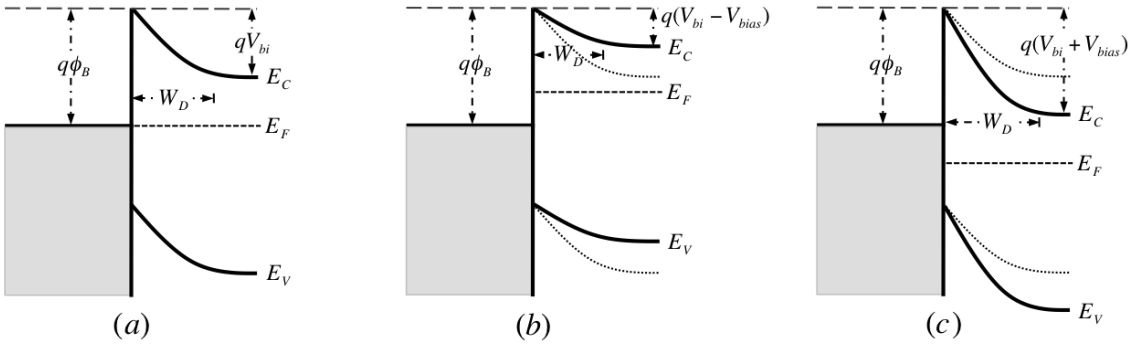


Figure 13. Metal/Semiconductor Junction under (a) zero applied bias, (b) forward bias, and (c) reverse bias voltage regimes

When a reverse bias voltage is applied, the amount of charge belonging to these layers increases, which is accompanied by an increase in the depletion width and the barrier height of the junction (see Figure 13), which greatly decreases current flow. Under forward bias conditions, the barrier height and depletion width are lowered, encouraging higher current densities. An expression for the non-equilibrium depletion width of the junction as a function of applied bias voltage is given by

$$W_D = \sqrt{\frac{2\varepsilon_S}{qN_D}\left(V_{bi} - V_{bias} - kT/q\right)} \tag{36}$$

where the sign convention for V_{bias} is positive for forward bias voltages and negative for reverse bias voltages. Substituting equation 36 into equation 4 yields an expression for the depletion capacitance per unit area of a metal/semiconductor junction under non-zero bias voltage:

$$C = \frac{\varepsilon_S}{W_D} = \sqrt{\frac{q\varepsilon_S N_D}{2\left(V_{bi} - V_{bias} - kT/q\right)}} \tag{37}$$

In order to calculate N_D for the semiconductor, equation 37 can be manipulated into the form

$$\frac{1}{C^2} = \frac{2(V_{bi} - V_{bias} - kT/q)}{q\varepsilon_S N_D} \tag{38}$$

Assuming the doping concentration N_D is uniform throughout the depletion region, plotting $1/C^2$ versus V_{bias} under reverse bias conditions should result in a linear relationship with a slope equal to

$$\frac{d(1/C^2)}{dV_{bias}} = -\frac{2}{q\varepsilon_S N_D} \tag{39}$$

From equation 39, the dopant concentration may be obtained. If plotting $1/C^2$ versus V_{bias} does not yield a straight line, this could mean that the doping concentration is not uniform throughout the depletion region, or (in the case of extremely thin films) that the width of the depletion region actually exceeds the thickness of the semiconductor thin film. In such cases, other methods must be utilized in order to quantify the dopant concentration. When applying the capacitance-voltage method to a p-n junction, N_D would be replaced with the term $N_A N_D/(N_A+N_D)$. If one side of the junction is more heavily doped than the other, the value obtained for the doping concentration represents the concentration on the more lightly doped side [35].

4.5 Dopant Concentration Characterization via Capacitance-Voltage Method

As a preliminary study to better understand electrical measurements of metal/semiconductor junctions in hopes of forming accurate equivalent circuit models of PLD-grown thin film structures, multiple configurations of commercial Schottky rectifying diodes were tested using EIS and the capacitance-voltage method. A diagram of one such configuration of two rectifying silicon diodes of different dopant concentrations connected

in series is shown in Figure 14a with corresponding dopant concentrations extracted via the capacitance-voltage method. It is clear that the diodes illustrated are connected with opposing polarities, which when under an applied bias as shown in Figure 14b, results in one diode under forward bias conditions and the other under reverse bias conditions. This configuration allows for selective electrical characterization of the dopant concentration of the junction in reverse bias. This preliminary study provided important insight to potential thin film structures with multiple junctions that otherwise would not have been easily discerned.

Considering the importance of the quality of metallic contact deposition for electrical measurements on semiconductor thin films, a subsequent study was performed with two objectives in mind: (1) to test various methods of metallic contact deposition onto a single crystal silicon wafer of known dopant species and concentration, and (2) to verify

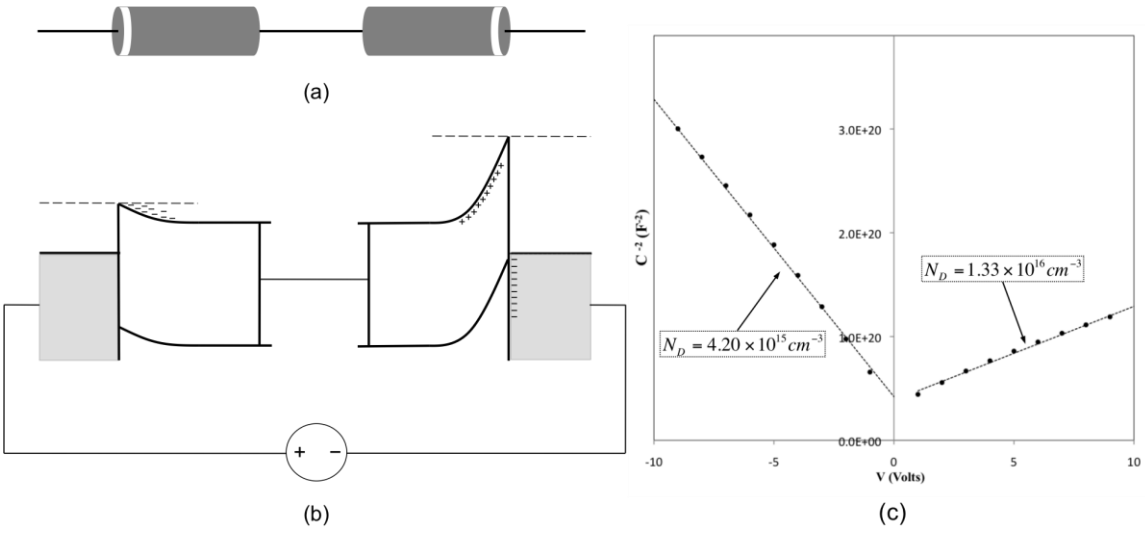
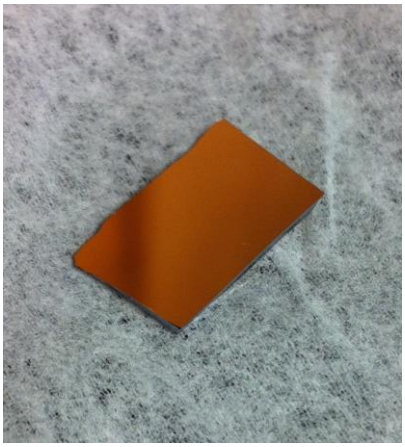


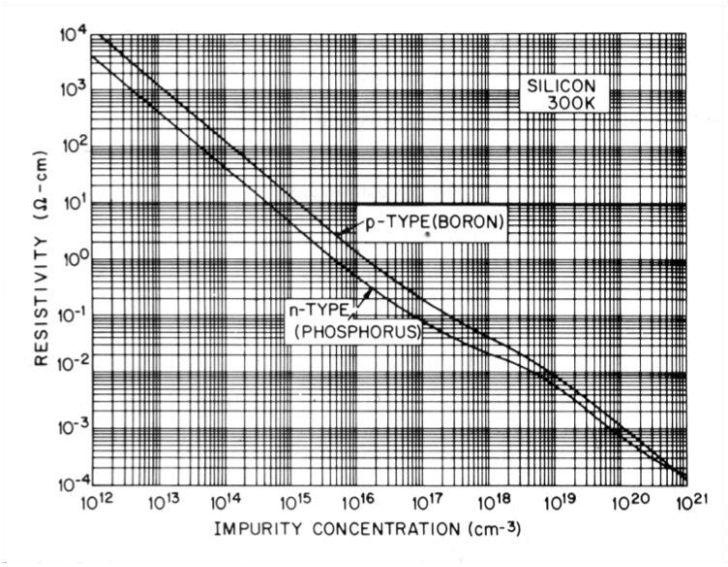
Figure 14. (a) Schematic illustrating NTE579 and NTE573 Schottky rectifying diodes wired in series with opposing polarities, (b) corresponding band structure showing junctions in forward bias (left) and reverse bias (right) regimes, and (c) resulting measurement of $1/C^2$ versus V_{bias} with corresponding dopant concentrations extracted from respective slopes using equation 35

the accuracy and consistency of the values of dopant concentration obtained using the capacitance-voltage method (under the abrupt approximation).

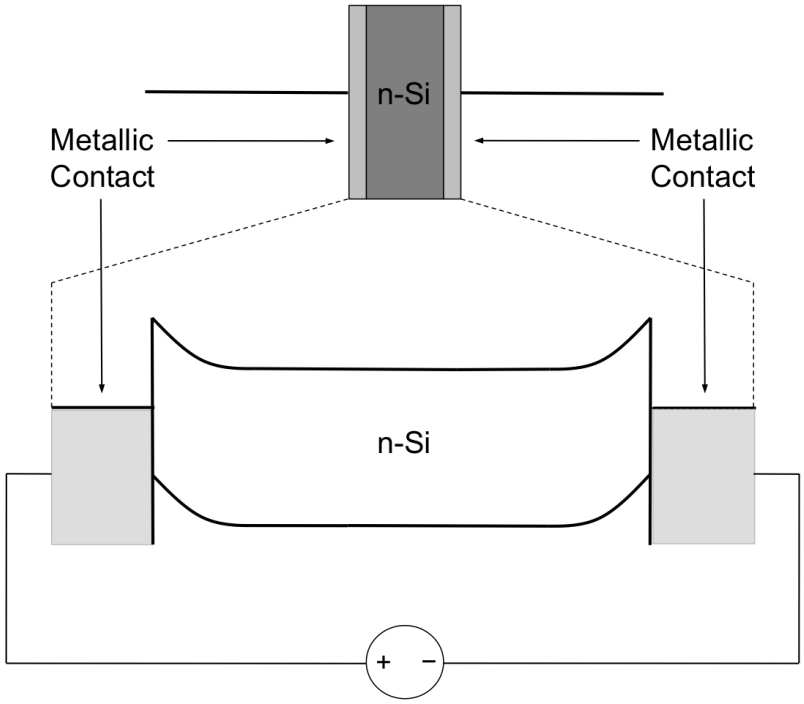
The contact deposition methods and materials tested include copper contacts deposited via PLD and silver contacts fabricated using a conductive silver-based paint utilizing various application techniques. Examples of the parameters varied within the study of application techniques for the silver-based paint include coating the entire surface of the wafer versus applying only a small circular drop, and simple air-drying of the contact versus heat treatment on a hot plate (50 – 90 °C) for 30 minutes. Contacts were deposited onto each sample in a symmetric fashion, with the front and back contact deposited in a consistent manner for an individual sample. Each sample was analyzed via EIS and capacitance-voltage measurements were performed to determine the dopant concentration of the silicon wafer.

Values of resistivity for thermal treatment of the contact/wafer samples on a hot plate under various temperatures ranging the silicon wafer were extracted for each sample using the measured dopant concentrations in conjunction with empirical data relating dopant concentration to resistivity of phosphorus-doped silicon samples [37] (see Figure 15b). Since each sample has two metal/semiconductor junctions (see Figure 15c), it was possible to extract a value for dopant concentration using each junction when in reverse-bias, which yielded two measured values per sample. As there were 18 total samples with contacts deposited using various different methods, 32 total values of dopant concentration were measured for the silicon wafer and are displayed in Figure 16b. It is noteworthy to mention that all methods used to deposit metallic contacts in this preliminary study resulted in measured dopant concentrations and corresponding values of resistivity that fell within





(a) (b)



(c)

Figure 15. (a) Actual image of silicon wafer with pulsed laser-deposited copper contacts used in this study; (b) Plot of resistivity versus dopant concentration of doped silicon samples [37] used to correlate measured dopant concentrations to resistivity values for comparison with known resistivity provided by wafer manufacturer; (c) Schematic illustrating basic structure of fabricated samples used in preliminary study of contact deposition methodology and corresponding energy band diagram

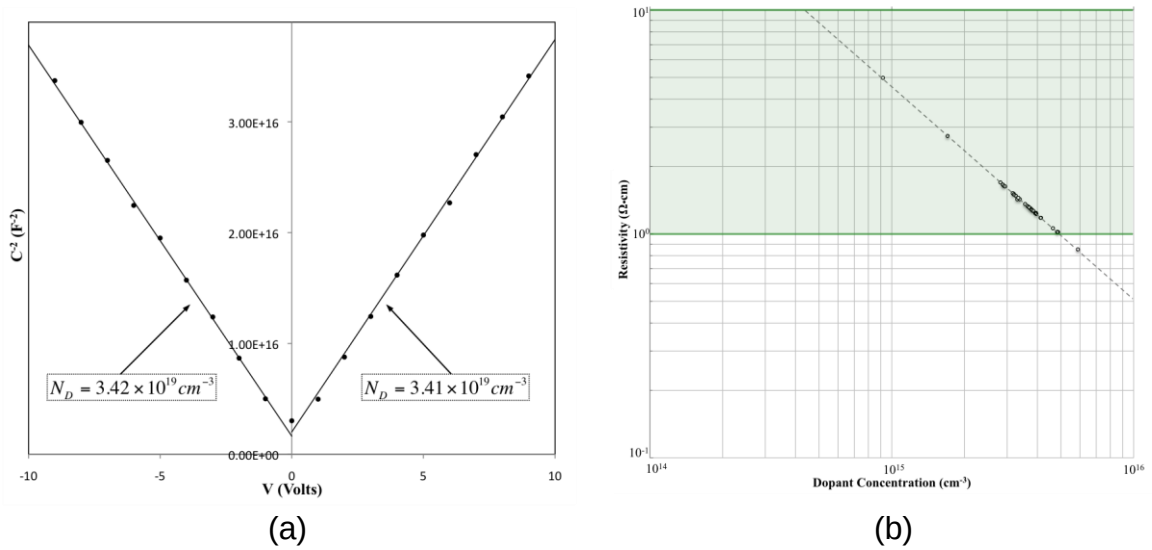


Figure 16. (a) Plot displaying $1/C^2$ versus applied bias voltage V on n-Si wafer with pulsed laser-deposited copper contacts with measured dopant concentrations using left and right junctions, and (b) plot displaying resistivity of n-Si wafer versus dopant concentration measured using capacitance voltage method on 18 samples utilizing various methods of metallic contact deposition (the region in-between the green lines represent accepted resistivity range provided by the wafer manufacturer)

uncertainty of the resistivity range provided by the manufacturer of the silicon wafer of 1−10 Ω•cm. These results provide confidence in the efficacy of the capacitance-voltage method for further applications to semiconductor thin films produced in this research that satisfy the same criteria assumed under the abrupt approximation.

4.6 Defect States at Metal/Semiconductor Interfaces

As seen in section 4.3, a potential barrier is formed when a metal and semiconductor make intimate contact due to the difference in the positions of the respective Fermi levels. If surface states of significant density are present at the semiconductor surface, a

depletion/accumulation region can be formed even before the metal/semiconductor junction is established. In order to assess methods of reducing resistances contributed by interfaces within thin film structures fabricated in this research and further pursue dissertation objectives (2) and (3), defect states arising at material interfaces must be explored. First studied in detail by Tamm [47] and Shockly [48], such surface states can arise when the periodic crystal potential is terminated on one side by a surface potential barrier. The source of the surface potential barrier can be impurity atoms, oxide layers, and/or structural imperfections at the surface. The energetic properties of the surface of the crystal will depend upon the density of surface states and their energy distribution [34]. Assuming an n-type semiconductor with acceptor states at the surface, electrons from donors near the surface will fill the empty surface states up to the Fermi level (assuming absolute zero), thus lowering the Fermi level near the surface (see Figure 17). This process creates a layer of negative charge at the surface, which in a similar manner to Schottky barrier formation, creates a space charge layer due to uncompensated donor ions. The degree of Fermi level lowering is magnified with higher surface state densities, which results in the creation of larger depletion regions and higher surface potential barrier heights.

The process of bringing together a metal and a semiconductor with a significant density of surface states can drastically change the interfacial band structure relative to the case of an ideal interface with no surface states. In cases of metal contact deposition on semiconductors with high surface state densities, the potential barrier formed at the junction is essentially independent of the metal work function [49]. Consider the case of a metallic contact being deposited onto an n-type semiconductor with a high density of

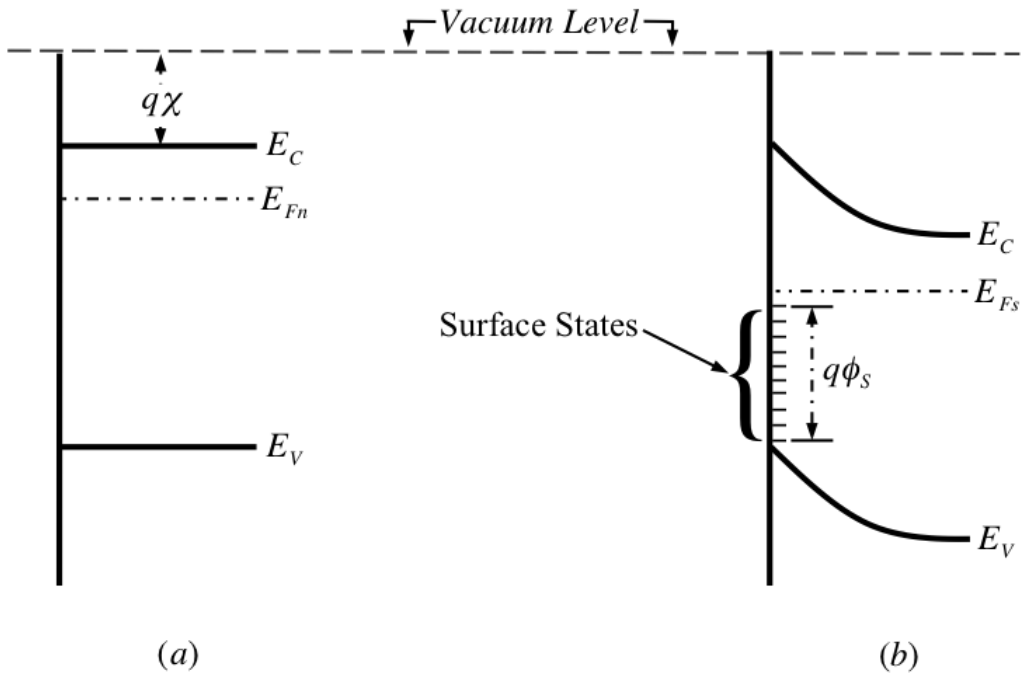


Figure 17. Band Diagrams of n-type semiconductor (a) with no surface states, and (b) with formation of depletion region and surface potential barrier due to presence of acceptor-type surface states

acceptor-type surface states, where the work function of the metal is smaller than that of the semiconductor (see Figure 18a). When the two materials are brought into contact in the absence of surface states, electrons leave the metal to fill states in the semiconductor in order to equalize the electric potential energies of the Fermi levels on both sides of the junction. As the Fermi level rises in the semiconductor, an accumulation layer is established (see Figure 18b), which does not possess the rectifying attributes of a depletion region with corresponding Schottky potential barrier. However, in bringing the same two materials together while accounting for the semiconductor surface states, electrons leaving the metal to bring the respective Fermi levels to equilibrium will first fill the surface states rather than states in the interior of the semiconductor.

If the density of surface states is high enough, these states will accommodate all the

electrons necessary to achieve equilibrium conditions. Recalling that the semiconductor develops a depletion region and potential barrier long before being brought into contact with the metal due to interaction between the surface states and the semiconductor interior (see Figure 17b), the junction at equilibrium consists of a depletion region instead of an accumulation region since very few (if any) electrons from the metal fill any states other than those at the surface during junction formation. Depending on the density of surface states, some electrons from the metal may occupy states in the interior of the semiconductor after the states at the surface have been filled. Even if this is the case, the junction still maintains the Schottky-rectifying depletion layer, but the barrier experiences some lowering ($\delta\phi$) due to the rise of the Fermi level near the interface [34].

The differences in this process with and without the effects of surface states are of particular relevance to this research because of the significant role that the density of surface states plays on potential barrier formation and charge transport behavior. Similar to the junctions described in Figure 18 and Figure 19, the n^+-GaAs/ZnSe interface is present in most of the thin film structures fabricated in this research, and it is clear that the density of surface states at this interface plays a significant role in the electrical properties and energetic profile of the associated potential barrier. Due to the drastic effect of surface states on each junction within the thin film structures of interest, effective and reproducible processes to decrease surface state densities at material interfaces were pursued and studied.

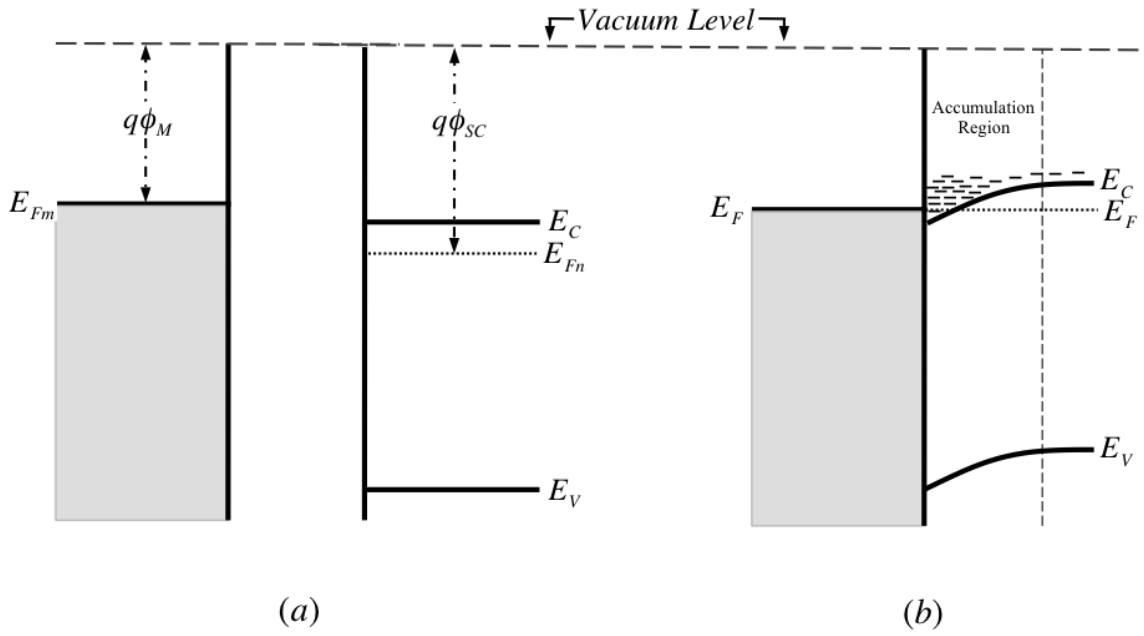


Figure 18. Energy Band Diagrams representing metal and n-type semiconductor (with $q\phi_{SC}>q\phi_M$) in the absence of surface states (a) before junction is established and (b) after junction formation and equilibrium achieved

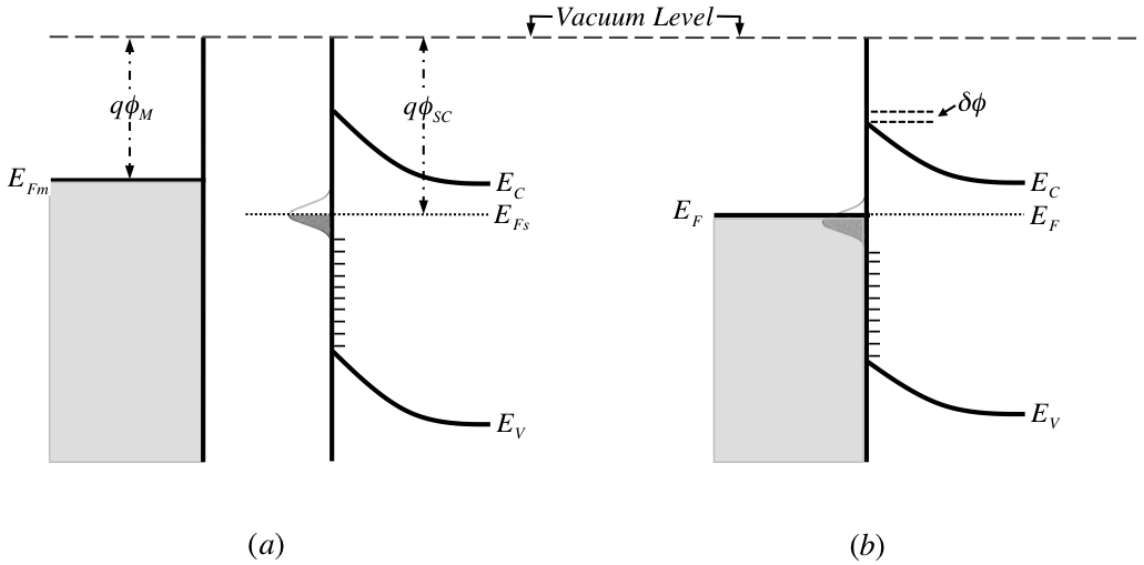


Figure 19. Energy Band Diagrams representing metal and n-type semiconductor (with $q\phi_{SC}>q\phi_M$) with surface states (a) before junction is established and (b) after junction formation and equilibrium achieved

4.7 Metallic Contact Annealing Process

Of the various interfaces present throughout the thin film structures produced for this research, a key interface of interest, due to its innate rectifying qualities, is the metal/semiconductor interface between the nickel contact and ZnSe-based thin films. Resolving contributions from metal/semiconductor junctions within multilayered thin films structures and realizing methods of controlling such contributions are significant milestones for achieving dissertation milestones (2) and (3). After crystallographic analysis was performed on each sample, Ni contacts were deposited onto both sides of each sample via a Magnetron Sputtering system. Each sample was loaded into the sputtering deposition chamber and pumped down to ~100 mtorr and then backfilled with Argon gas to achieve ~200 mtorr background pressure. A plasma plume was initiated using a high voltage source for 60 seconds, which resulted in a conductive Ni film coating the entire surface of the sample. To prevent electrical shorting, the edges of each sample were cleaved after contact deposition.

After depositing metallic contacts, electrochemical impedance spectroscopy (EIS) was performed to obtain Nyquist plots and current-voltage measurements for each sample. It is well known that when a metal and semiconductor are brought into intimate contact, a Schottky barrier is formed at the interface. According to the Schotkky model, the limiting value of this barrier can be calculated by taking the difference of the work function of the metal and electron affinity of the semiconductor [35]. Taking the work function of Ni to be 5.01 eV and the electron affinity of ZnSe to be 4.06 eV [54], the limiting value of the potential barrier formed at a Ni/ZnSe interface should be ~1 eV based on the Schottky model in the absence of surface states. The addition of high surface state densities at the

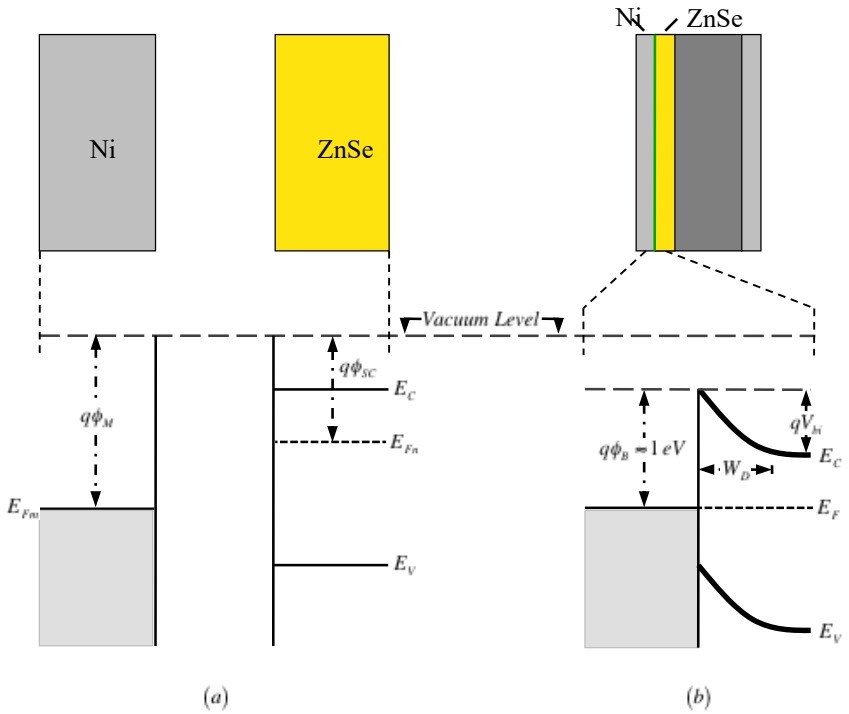


Figure 20. Schematic showing band diagrams (a) before and (b) after Ni/ZnSe junction formation in the absence of surface states

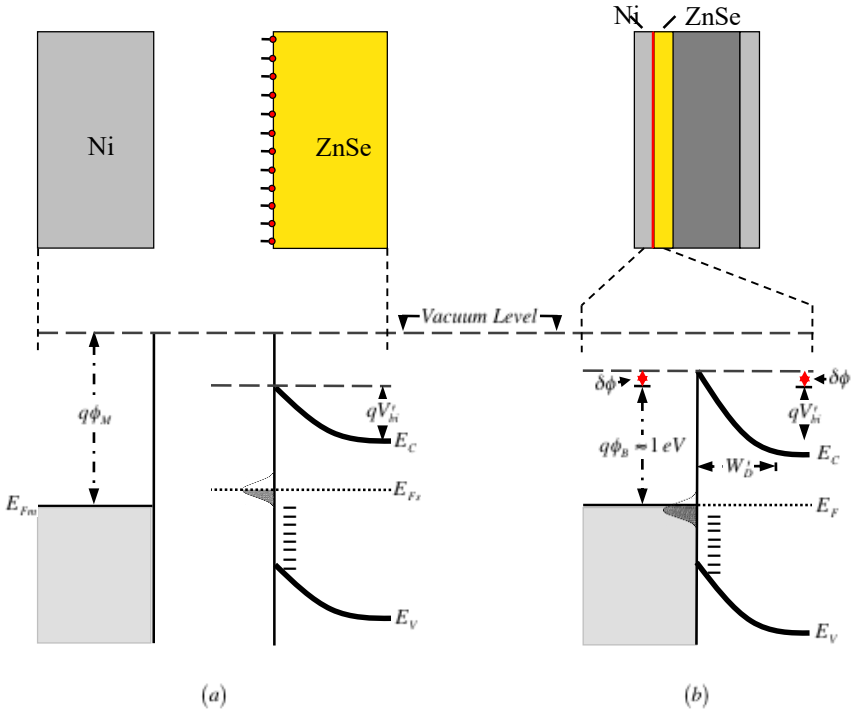


Figure 21. Schematic showing band diagrams (a) before and (b) after Ni/ZnSe junction formation accounting for high density of surface states at ZnSe surface

ZnSe surface increases this barrier height (see Figures 20 & 21), which further inhibits charge transport across the junction. In order to decrease the effects of the potential barrier for both the Ni/GaAs and Ni/$ZnS_{0.1}Se_{0.9}$ interfaces with hopes of maximizing achievable current densities, each sample underwent an annealing process in forming gas background (5% H_2 in N_2) maintained at ~60 torr above atmosphere at 300°C for 5 minutes [55]. Upon completion, the samples were allowed to cool to room temperature while the forming gas background was maintained. EIS measurements were obtained before and after the annealing process for each sample to observe the effects of the process on each sample's electrical properties. EIS measurements were also obtained for the GaAs substrate alone to aid in extracting electrical properties of the more complicated thin film structures of the other samples. For the Ni/GaAs/Ni structure, the plot of current density versus applied voltage displayed a nonlinear trend in the data.

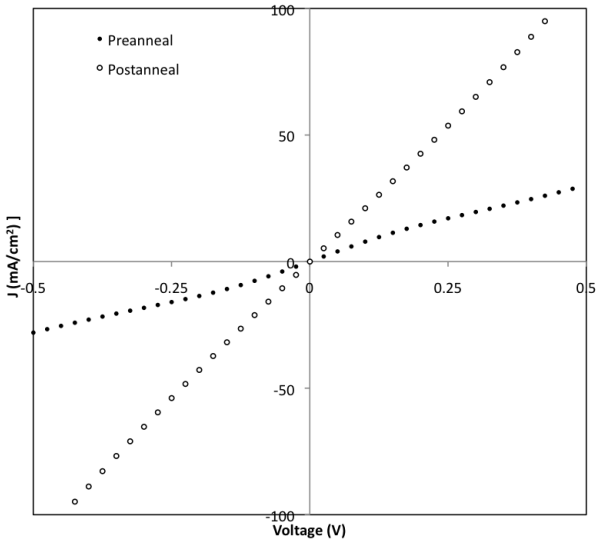


Figure 22. Plot of current density versus applied bias voltage for Ni/GaAs/Ni structure showing nonlinear preanneal behavior and ohmic postanneal behavior before the annealing phase

After annealing, the sample displayed behavior indicative of an ohmic junction (see Figure 22), which indicates possible passivation of surface states and resulting lowering of the potential barrier at the interface.

CHAPTER 5

EPITAXIAL GROWTH OF Cr^{2+}:ZnSe AND ZnS_xSe_{1-x} THIN FILMS BY PULSED LASER DEPOSITION

5.1 Introduction

The success of blue-green light emitting devices developed with MBE-grown epitaxial multilayer ZnSe-based structures suggests that the best route for an efficient mid-IR device as illustrated in Figure 1 would also be an epitaxial structure. In the case of our mid-IR active materials, MBE has not been a viable crystal growth approach because of the prohibitive high costs of dedicating an MBE system for TM ion doping. Pulsed laser deposition, however, is in principle capable of delivering quality epitaxial materials and has demonstrated Cr^{2+}:ZnSe with good emission in the mid-IR. Accordingly, we have made a substantial investment of time and effort to grow key elements of the structure of Figure 1 using PLD.

5.2 Growth of ZnS_xSe_{1-x}

Our first effort at epitaxy involved the ternary alloy ZnS_xSe_{1-x}, which was chosen for its suitability for lattice-matched epitaxial growth relative to the GaAs substrate. Incorporating sulfur (S) into the ZnSe lattice decreases the lattice parameter, and reaches

lattice-matching conditions with GaAs when x=0.06 [69]. This material is of significance to a potential multilayered mid-IR lasing device in that it could serve as a guiding layer of the optical field confined by an adjacent layer of lower index of refraction. With the incorporation of the appropriate dopants, ZnS_xSe_{1-x} is of further significance to the structure by providing charge injection into the active Cr^{2+}:ZnSe layer. Epitaxial growth of each layer is desired to achieve the electronic and optical properties necessary for successful integration into a multilayered lasing device, and objective (1) of this dissertation involves investigating factors related to the feasibility and limits of PLD epitaxy, as well as the crystalline quality of material layers. Therefore, a careful study was conducted on the effects of varying S content and growth temperature on the crystal quality of the resulting thin films.

To the best of our knowledge, this research is the first instance of the ternary alloy, ZnS_xSe_{1-x}, being grown my means of PLD. Our strategy for growing epitaxial thin films by PLD began with the preparation of several ablation targets that were produced in-house by mixing the appropriate masses of ZnSe and ZnS powders, pressing the mixture in a hydraulic press at 5000 psi, sealing the compressed pellet in an evacuated quartz ampoule at ~10 mtorr, and placing the sealed ampoule inside a furnace to anneal at 950°C for 3 days. This process produced a solid, ceramic target, suitable for ablation, in the PLD chamber. ZnS_xSe_{1-x} targets with compositional parameters of x=0.02, 0.06, and 0.10 were produced. Several experimental parameters are expected to impact the process of epitaxial growth, including the sulfur concentration of the target, growth temperature, and laser energy density used during deposition. In order to optimize the conditions for epitaxial growth of the ZnS_xSe_{1-x} layers inside the multilayered structure, the sulfur concentration was varied

for 3 different ablation targets, and films were deposited for various substrate temperatures (400°C, 425°C, 450°C) using each of the 3 targets. Each film was deposited onto an n-type GaAs (100) substrate that was cleaned and chemically etched for native oxide removal before each deposition by sonicating in acetone, methanol, and trichloroethylene (each for 10 minutes), and then submerging in a 3:1 H_2O:HCl solution for 1 minute to remove any existing oxide layer [38]. The substrate was then immediately loaded into the vacuum chamber and left to pump down to a base pressure of ~10^{-6} torr. Once this pressure was attained, the substrate heating process was initiated until the intended deposition temperature was reached. For each deposition, the laser energy density (2 J/cm^2), frequency of ablation (10 Hz), and number of pulses (2500) were kept constant while the substrate temperature and ablation target composition were varied.

5.3 Crystallographic and Compositional Characterization

Each film was characterized for crystallographic orientation and crystal quality by X-ray diffraction (XRD) analysis, and the approximate chemical composition was assessed by energy dispersive X-rays (EDX). As was expected due to stoichiometric preservation from target to film characteristic of PLD, an increase in sulfur concentration of the films is consistently observed with increasing compositional parameter, *x*, of the respective ablation target used for deposition (see Figure 23). Of all the films that were deposited of ZnS_xSe_{1-x} at varying compositional parameters and substrate temperatures, epitaxial characteristics were observed in films deposited under specific experimental conditions, while other deposition regimes resulted in thin films displaying unmistakable

polycrystalline features (see Table 1a). As a preliminary test for epitaxy, a 2θ XRD scan was performed on each of the films. Several films exhibited diffraction peaks extraneous to that of the GaAs substrate, indicative of a polycrystalline film structure.

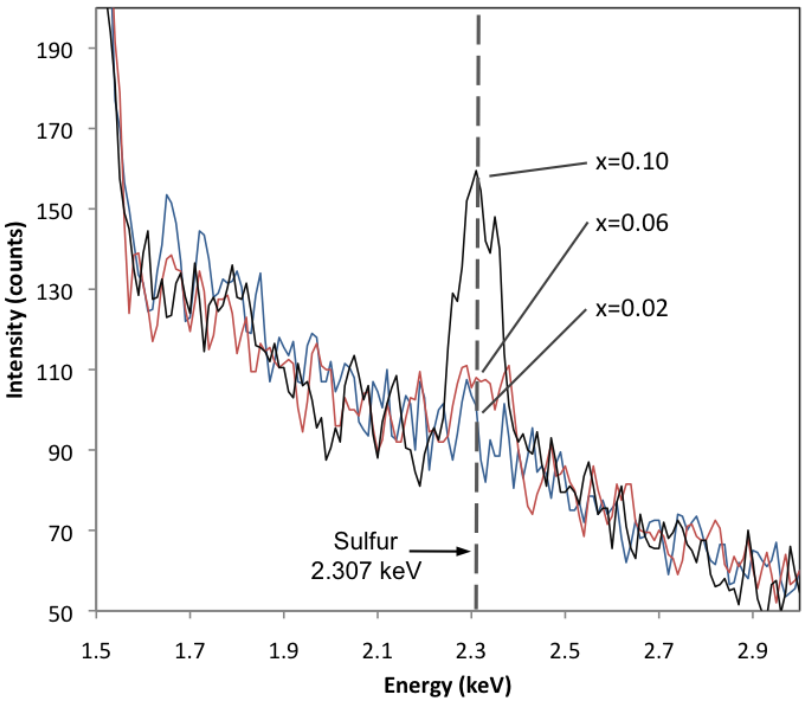


Figure 23. Energy dispersive X-ray spectra showing relative intensities of sulfur peak in ZnS_xSe_{1-x} thin films for varying x (reproduced from [12] with permission © 2016 *MRS Proceedings*)

However, some films exhibited no diffraction peaks in the XRD 2θ scan data except that independently displayed by the substrate (see Figure 24). To further test the films for epitaxy, symmetric 2θ/ω scans were performed on each film to look for extraneous peaks to the substrate in this geometry. For films displaying no additional peaks other than the (h00) group of substrate peaks (further indication of epitaxy), rocking curves about the (400) substrate peak were performed to characterize the films for differences in lattice parameters and dislocation density [39].

Table 1a. Combinations of Varied Deposition Parameters and Resulting Crystallographic Features of ZnS_xSe_{1-x}/GaAs Thin Films as indicated by XRD Data

		Deposition Temperature (°C)		
		400	425	450
Sulfur (S) At. %	0.02	Polycrystalline	Polycrystalline	Epitaxial
	0.06	Polycrystalline	Polycrystalline	Epitaxial
	0.10	Polycrystalline	Epitaxial	Polycrystalline

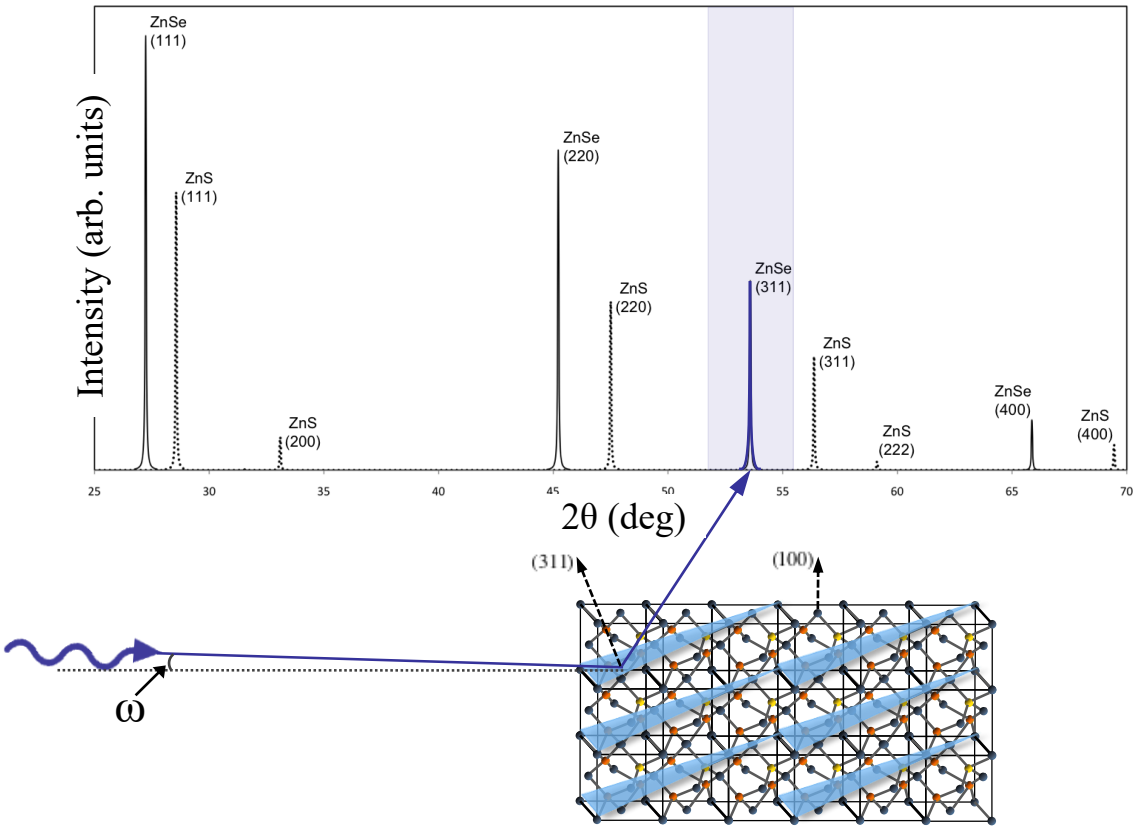


Figure 24. Schematic illustrating XRD 2θ glancing angle scan behavior for epitaxially grown ZnSSe films atop GaAs substrates showing a singular diffraction peak due to ZnSe/GaAs (311) lattice planes

5.4 Pseudo-Voigt Profiling

Pseudo-Voigt profiles were fit to both the film and substrate diffraction peaks to aid in film analysis. The pseudo-Voigt profile is a weighted sum of Gaussian and Lorentzian functions given by [40]

$$f_{pV}(x) = (1-\eta) f_G(x;\gamma_G) + \eta f_L(x;\gamma_L) \tag{40}$$

where $f_G(x;\gamma_G)$ and $f_L(x;\gamma_L)$ are the normalized Gaussian and Lorentzian functions with full width at half maximum (FWHM) given by

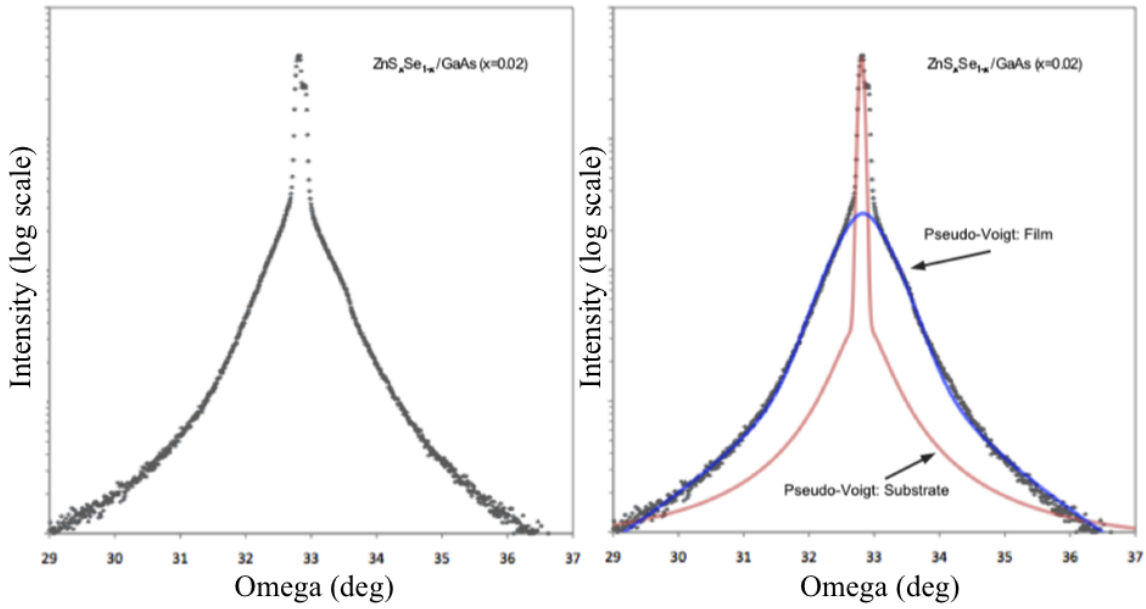
$$\Gamma = 2(\ln 2)^{1/2}\gamma_G = 2\gamma_L \tag{41}$$

Figure 25 shows the raw data on the left along with the same data with added pseudo-Voigt fits on the right. The pseudo-Voigt for the substrate was fit to the Cu $K\alpha_1$ (1.5406 Å) diffraction peaks even though both $K\alpha_1$ and $K\alpha_2$ peaks were present in all scans.

Since structural defects significantly contribute to broadening of the rocking curve FWHM, their concentration can be inferred using the width of the XRD rocking curves. In the case of epitaxial growth of ZnSe-based alloys on GaAs, it is well established from transmission electron microscopy (TEM) studies that the dominant structural defect are 60° dislocations [42]. Following the pioneering work of Ayers et al. [41], an upper bound for the dislocation density *D* can be found using the expression

$$D = (\Delta\omega)^2 / 4.36b^2 \tag{42}$$

where Δω is the FWHM of the rocking curve, and **b** is the Burgers vector associated with the 60° dislocations. All films produced in this research are expected to be relaxed as their thickness (~300 nm) likely exceeds the critical thickness for the ZnSe/GaAs system, which lies somewhere between 100-220 nm depending on growth conditions [43–46]. As seen in Fig. 25, the substantial width of the film peaks observed in our data results in the



(a) (b)

Figure 25. XRD rocking curve of ZnS_xSe_{1-x} for x=0.02 and 450°C (a) with raw data only and (b) with pseudo-Voigt fits for both film and substrate for comparison (reproduced from [12] with permission © 2016 *MRS Proceedings*)

superposition of film and substrate peaks, which requires careful inspection for correct interpretation.

XRD rocking curves were obtained for each of the epitaxial films, and a variation in the FWHM and peak shift between film and substrate (indicative of the difference in lattice parameter between the epilayer and the substrate) was observed as a function of the location of the x-ray spot. Figure 26 shows rocking curves performed at various locations across the surface of the film, and displays the corresponding values of dislocation density (D) and difference in lattice parameter ($\Delta a/a$) determined from data collected at each location. Assuming the thickness of the film takes on an approximate Gaussian profile (see Figure 26), spot locations were chosen corresponding to locations of maximum film thickness (spot location #1), intermediate film thickness (spot location #2), and minimum film thickness (spot location #3). The Bragg relation was used to

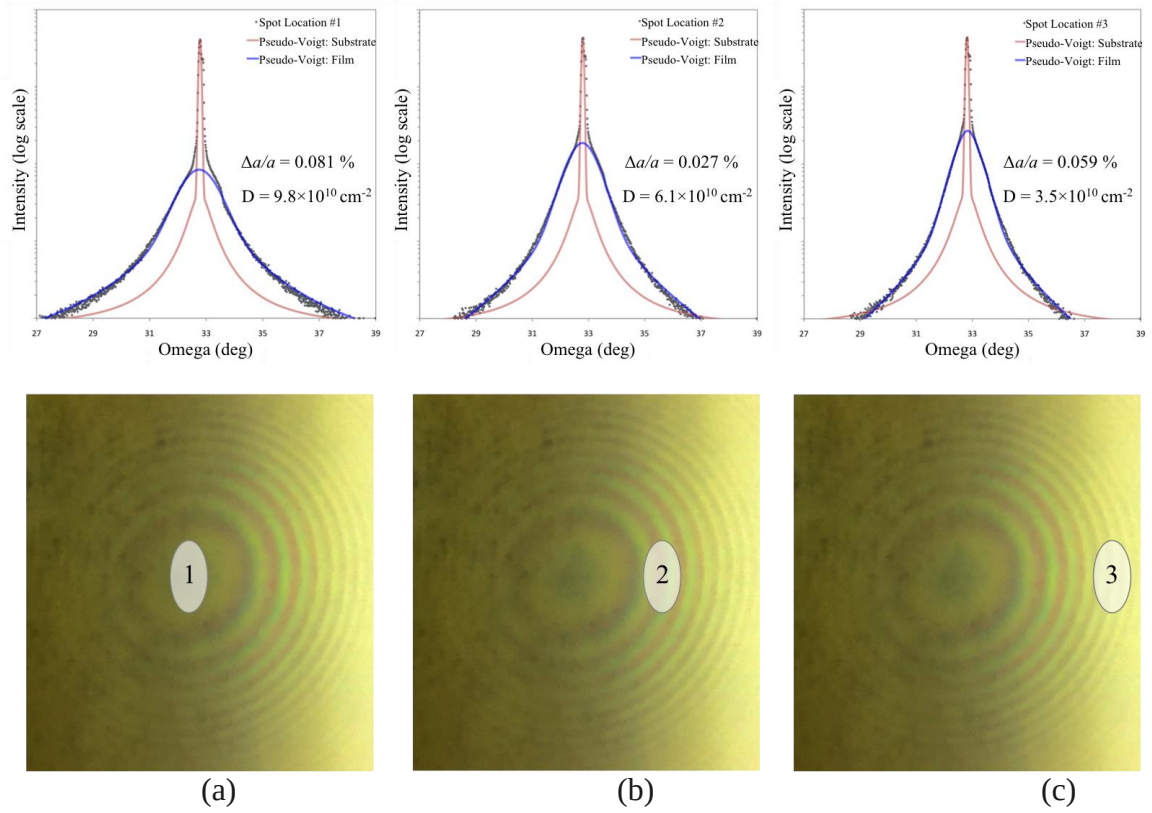


Figure 26. XRD rocking curves about (400) plane for a single epitaxially-oriented ZnS_xSe_{1-x}/GaAs (x=0.02) film grown at 450°C showing variation in dislocation density and relative peak shift between film and substrate as a function of the location of the x-ray spot during data collection for spot locations (a) #1, (b) #2, and (c) #3

determine lattice parameters and resulting differences in lattice parameter between substrate and deposited film and is given by

$$2d\sin\theta = n\lambda \tag{43}$$

where d is the interplanar spacing of the crystal lattice (referred to elsewhere in this chapter by the symbol "a"), n is a positive integer, λ is the wavelength of incident x-ray radiation (1.5406 Å), and θ is the scattering angle relative to the surface. Since the crystals grown in this research are all cubic in nature, obtaining the lattice parameter in this manner is appropriate.

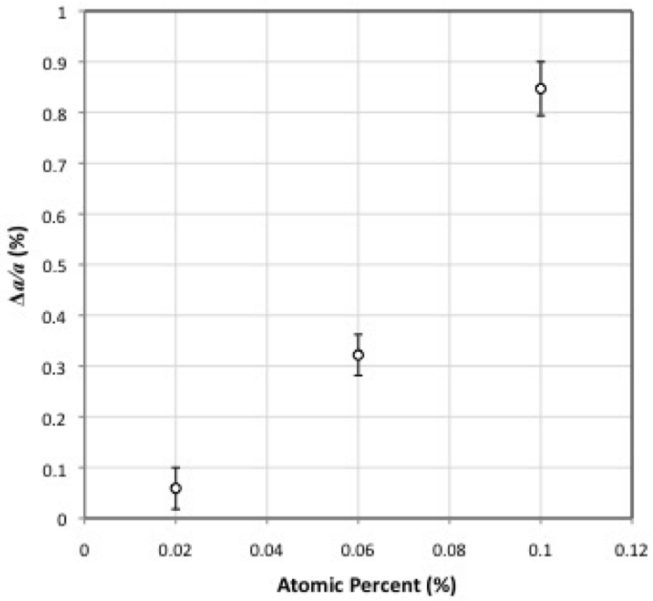


Figure 27. Plot of average percent difference in lattice parameter of GaAs substrate and ZnS_xSe_{1-x} film versus nominal atomic percent (x) of Sulfur present in film

Table 1b. Nominal Growth Parameters and Averaged Crystallographic Properties of Epitaxially-oriented ZnS_xSe_{1-x}/GaAs Thin Films

Sulfur (S) Atomic %	Growth Temperature (°C)	$\tilde{a}_{GaAs}$ (Å)	$\tilde{a}_{ZnSSe}$ (Å)	$\Delta\tilde{a}/\tilde{a}_{GaAs}$ (%)	$\tilde{D}$ (cm^{-2})
0.02	450	5.6889	5.6899	0.017	6.48×10^{10}
0.06	450	5.6292	5.6473	0.322	2.87×10^{10}
0.10	425	5.6978	5.6496	0.847	1.01×10^{11}

The epitaxially-oriented x=0.02 / 450°C sample showed an increase in determined values of lattice parameter of the ZnSSe film (relative to the GaAs substrate) and dislocation density with increasing thickness of the x-ray spot location on the film surface. This indicates that as regions of the ZnSSe film increase in thickness at different rates during growth, there is a non-uniform degree of relaxation of the lattice structure. In areas of high thickness, the dislocation density is measured to be higher than in thinner regions where the film may still be partially under strain from lattice-matched growth atop the

GaAs substrate. As the film exceeds the critical thickness in each respective region, the localized structures can no longer hold the increasing amount of strain, resulting in lattice relaxation and subsequent formation of stacking faults and dislocations.

While all 3 epitaxially-oriented films displayed this trend with variable thickness, an increase in the average percent difference in lattice parameter between film and substrate was observed with increasing sulfur concentration (see Figure 27). Contrary to our expectations due to well established lattice-matching conditions of ZnS_xSe_{1-x} (x=0.06) on GaAs [69], the sample with x=0.06 did not display the lowest average difference in lattice parameter between the film and substrate. However, this sample did display the lowest average density of structural defects across the film, suggesting that this film contained fewer stacking faults and dislocations than both the x=0.02 / 450°C and x=0.10 / 425°C epitaxially-oriented samples (see Table 1b).

A possible explanation for the disparity between measured values of the dislocation density and difference in lattice parameters of film and substrate is an inhomogeneous distribution of S atoms throughout the film structure during growth. Considering the known lattice parameter of GaAs (5.6535 Å) is just under that of ZnSe (5.6686 Å) and larger than that of ZnS (5.4093 Å) [23], non-uniform S concentrations within the films could explain the observed misalignment between measured values of dislocation density and relative lattice parameters of film and substrate. Furthermore, it appears that the incorporation of S into the ZnSe lattice changes the growth dynamics with increasing S (as a drop in the growth temperature for epitaxial growth was observed for x=0.10), which could also account for the inconsistent behavior of measured values of

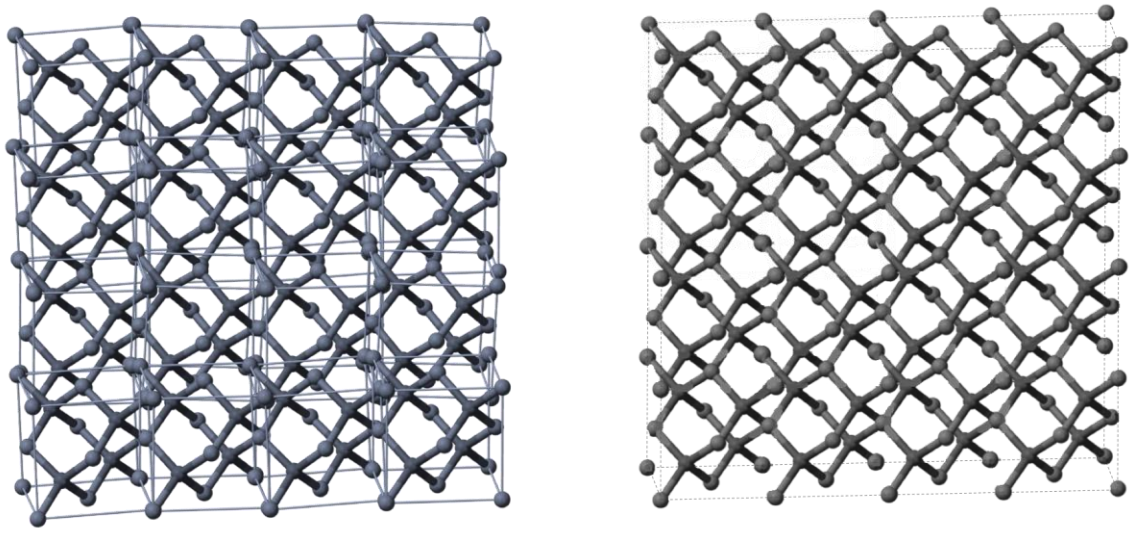


Figure 28. Diagram illustrating cubic ZnSe material with (a) epitaxially-oriented vs. (b) single crystal lattice structure

lattice parameter difference and dislocation density as a function of increasing sulfur incorporation.

Although these 3 thin films are clearly epitaxially-oriented with respect to the (100)-oriented GaAs substrate, they are unlikely to represent single crystals as illustrated in Figure 28. As is typical in PLD-grown epitaxial films, factors such as high densities of structural defects, the observed variation in measurements of lattice difference Δa, and structural defect density dependent on the location of the x-ray spot during data collection, all suggest highly textured, epitaxially-oriented thin films with some level of polycrystallinity in the layers. This conclusion is corroborated by the electrical properties reported in chapter 6, which even for epitaxially-oriented films, show significant features associated with polycrystals.

5.5 Crystallographic Properties of Cr^{2+}:ZnSe/ZnS_xSe_{1-x} Structures

In pursuit of further progress towards dissertation objective (1), a series of thin film structures was deposited to study the effect of the addition of a layer of ZnSe at the GaAs/ZnS_xSe_{1-x} interface. To simultaneously direct our efforts towards dissertation objective (2), Cr^{2+}:ZnSe was chosen as the interfacial layer material for this study in order to investigate the corresponding electrical properties in a multilayered structure as a function of thickness and crystal quality of the layers. Several multilayered thin film samples were produced for this study with the structure illustrated in Figure 29, and the respective thicknesses of the various material layers are listed in Table 2.

When ZnS_xSe_{1-x} is grown directly onto the GaAs surface, S atoms interact with Ga and As atoms on the GaAs surface to produce stacking faults within the ZnS_xSe_{1-x} layer [50-52]. To reduce the density of stacking faults, a thin ZnSe layer utilized as a buffer layer between the GaAs and ZnS_xSe_{1-x} layer has been shown to result in deposited film structures of higher crystallinity and lower density of structural defects, making them less prone to device failure [50,53]. In an effort to achieve thin film structures of higher crystallinity with mid-IR electroluminescence in mind, the effects of depositing an additional Cr-doped ZnSe layer of various thicknesses at the GaAs interface were studied with two major thrusts in mind: (1) to eventually integrate an appropriate buffer layer into the multilayered structure concept shown in Figure 1 in order to achieve thin film structures of higher crystal quality, and (2) to investigate the impact of the thickness of the Cr^{2+}:ZnSe layer on the crystallographic and electrical properties of the structure, both of which are respectively aligned to dissertation objectives (1) and (2). For each sample produced in this study, identical parameters for the laser energy density (2 J/cm^2),

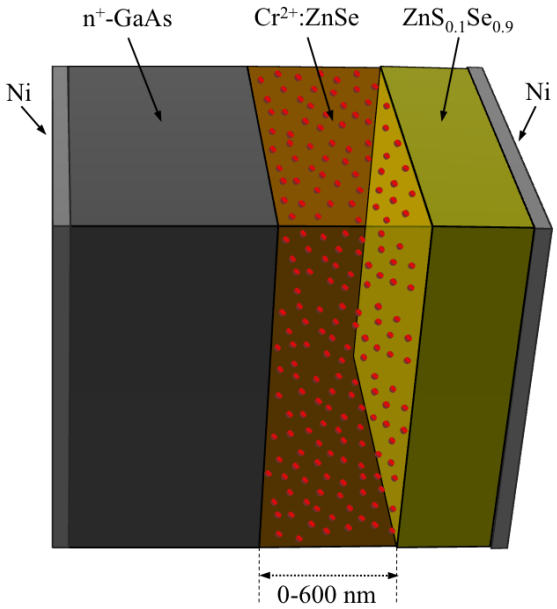


Figure 29. Diagram illustrating multilayered thin film structure with Cr^{2+}:ZnSe interfacial layer of variable thickness sandwiched between GaAs substrate and 300 nm $ZnS_{0.1}Se_{0.9}$ layer capped with Ni contacts on both ends

Table 2. Material Layer Thicknesses of Deposited Thin Film Structures

Structure	Thickness of $ZnS_{0.1}Se_{0.9}$ Layer (nm)	Thickness (*t*) of Cr^{2+}:ZnSe Interfacial Layer (nm)	Substrate
1	300	0 (no Cr^{2+}:ZnSe layer)	n-GaAs
2	300	150	n-GaAs
3	300	300	n-GaAs
4	300	450	n-GaAs
5	300	600	n-GaAs

frequency of ablation (10 Hz), growth temperature (450°C), and number of pulses (5000) were used for the deposition of the ZnS_xSe_{1-x} layer. The growth temperature of 450°C was chosen as it was discovered to produce a polycrystalline film in the previous study, and this provided the potential for a high degree of improvement of layer crystallinity due to the integration of the proposed Cr^{2+}:ZnSe layer. For samples incorporating the Cr^{2+}:ZnSe layer, an ablation target of Cr^{2+}:ZnSe with a nominal Cr concentration of 6×10^{19} cm^{-3} was

produced in-house and used to deposit layers of various thicknesses in between the GaAs substrate and ZnS_xSe_{1-x} layer.

Each film was characterized for respective crystallographic properties such as crystal orientation and defect density by XRD analysis, implementing both glancing angle 2θ scans and rocking curve scans to probe general crystal phase information and epilayer characteristics, respectively. Just as in the previous study, glancing angle 2θ scans were performed on each sample as a first step in distinguishing between epitaxial and polycrystalline features present in the XRD data. Even though the GaAs substrates used throughout this dissertation research were sphalerite, face-centered cubic (FCC) structures with a (100) oriented surface, the glancing angle 2θ scans coincidentally detect the (311) plane of the GaAs crystal (see Figure 30a). Therefore, for an epitaxially-oriented film atop this particular substrate, no other peaks except that of the (311) cubic plane should be observed in the glancing angle 2θ scan data (see Figure 30b). Figure 30 shows XRD glancing angle 2θ plots of the GaAs substrate, structure #2 (epitaxially-oriented), and structure #1 (polycrystalline) to illustrate these characteristics.

Of the samples produced for this study, only the $ZnS_{0.1}Se_{0.9}/Cr^{2+}$:ZnSe sample of thickness (nm) ratio 300:150 (structure #2) exemplified a singular peak on the glancing angle 2θ scan, while all other samples displayed extraneous peaks indicating polycrystalline structures. For structures #3-5, as the thickness of the Cr^{2+}:ZnSe layer was increased, a clear deviation from epitaxial orientation of the deposited layers was observed as intensities of secondary growth peaks increased relative to the primary growth peak observed in all samples. Extended studies of the polycrystalline structures will be expanded upon further in chapter 6.

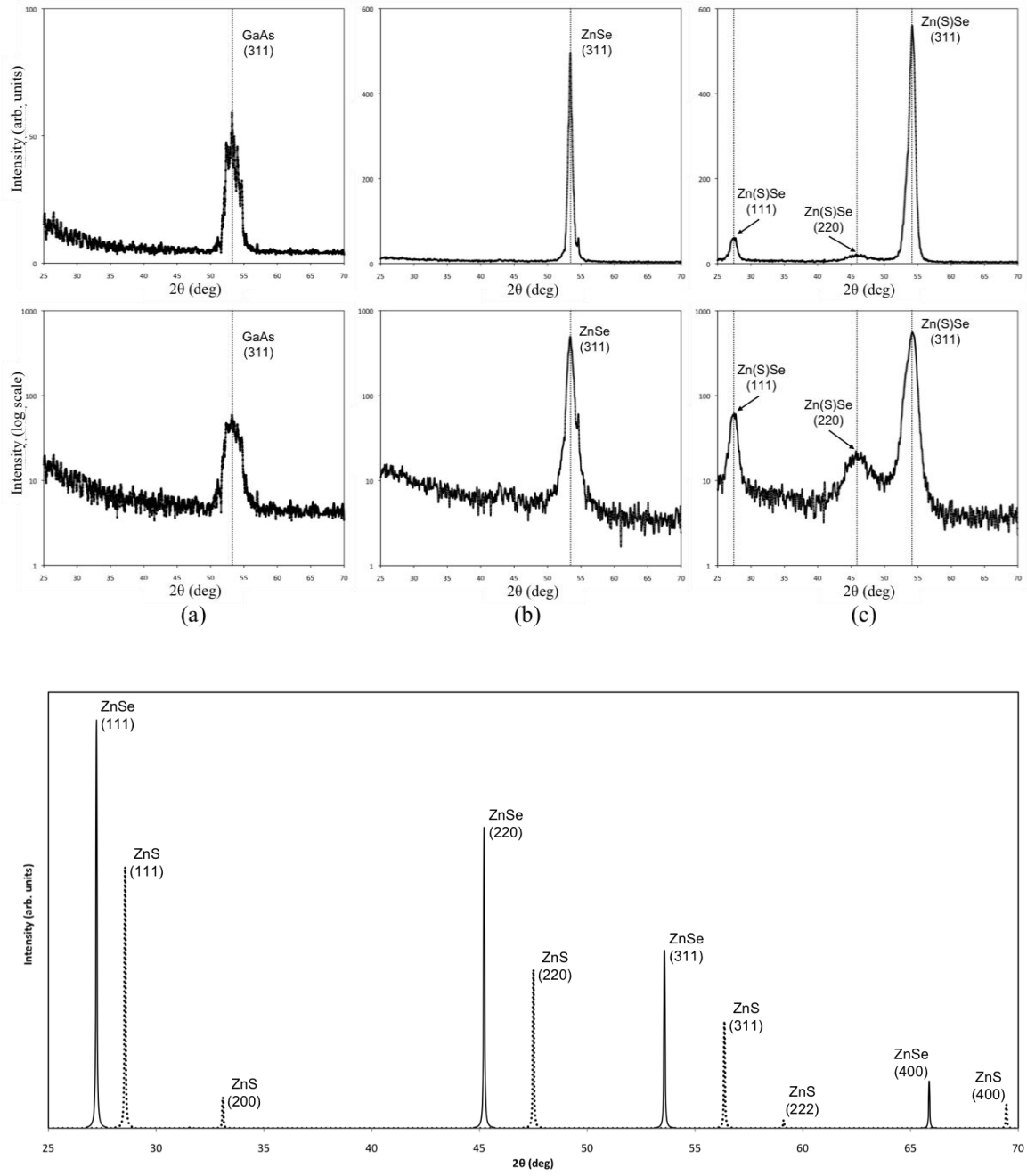


Figure 30. XRD Glancing Angle 2θ Scans displayed in linear (top row) and logarithmic scale (middle row) of (a) GaAs substrate, (b) structure #2, and (c) structure #1 showing a singular diffraction peak for substrate and structure #2 versus multiple diffraction peaks for structure #1, along with (d) standard diffraction patterns for ZnSe (cubic) and ZnS (cubic) for comparison

Similar to the study on ZnS_xSe_{1-x} thin films grown with variable compositional parameter and substrate temperature documented in the previous section, XRD rocking curves were performed to characterize the epitaxially-oriented structure for dislocation density and difference in lattice parameter with respect to the substrate. Pseudo-Voigt profiles were also fit to both the film and substrate diffraction peaks in the rocking curve data to aid in film analysis. Figure 31 shows XRD rocking curve plots of structure #2 of both the raw data along with the same data with added pseudo-Voigt fits. The pseudo-Voigt profiles for this study were also fit to the Cu $K\alpha_1$ (1.5406 Å) diffraction peaks in all scans. Even though glancing angle 2θ scan data for structure #1 displayed clear characteristics of a polycrystalline film structure, rocking curve scans were performed about the (400) growth peak on both structure #1 and structure #2 to obtain a qualitative comparison of the variation in defect density and differences in lattice parameters of the primary growth phase for an identical material ($ZnS_{0.1}Se_{0.9}$) grown atop GaAs, with and without the presence of the Cr^{2+}:ZnSe layer (see Figure 32). Once again, the Bragg relation was used to determine lattice parameters and resulting mismatch between substrate and deposited film.

Effective lattice parameters of the films were measured to be 5.6955 Å for structure #2 and 5.7188 Å for structure #1, resulting in differences in lattice parameters relative to the measured value for GaAs (5.6878 Å) of 0.136% and 0.545%, respectively. It is noteworthy to mention that the accepted value for the lattice parameter of Zinc-blende GaAs is 5.6535 Å, and the deviation observed in the measured values determined from the XRD rocking curve data throughout this chapter is due to the tilt of the sample relative to the plane parallel to the measurement surface. Since both the substrate and

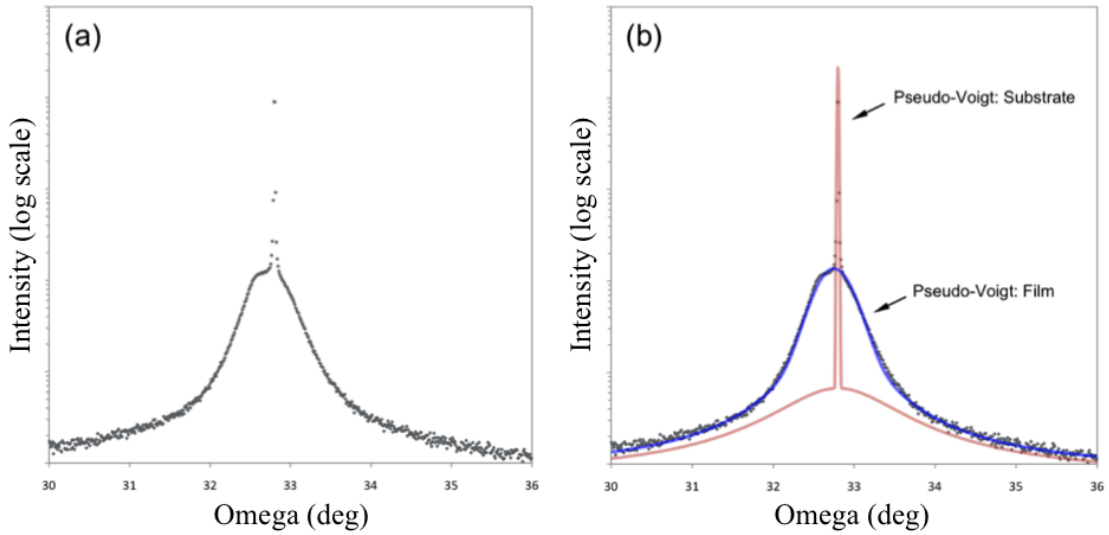


Figure 31. XRD rocking curve plots of $ZnS_{0.1}Se_{0.9}/Cr^{2+}$:ZnSe (300:150 nm thickness ratio) on GaAs with (a) raw data only and (b) with pseudo-Voigt fits for both film and substrate for comparison

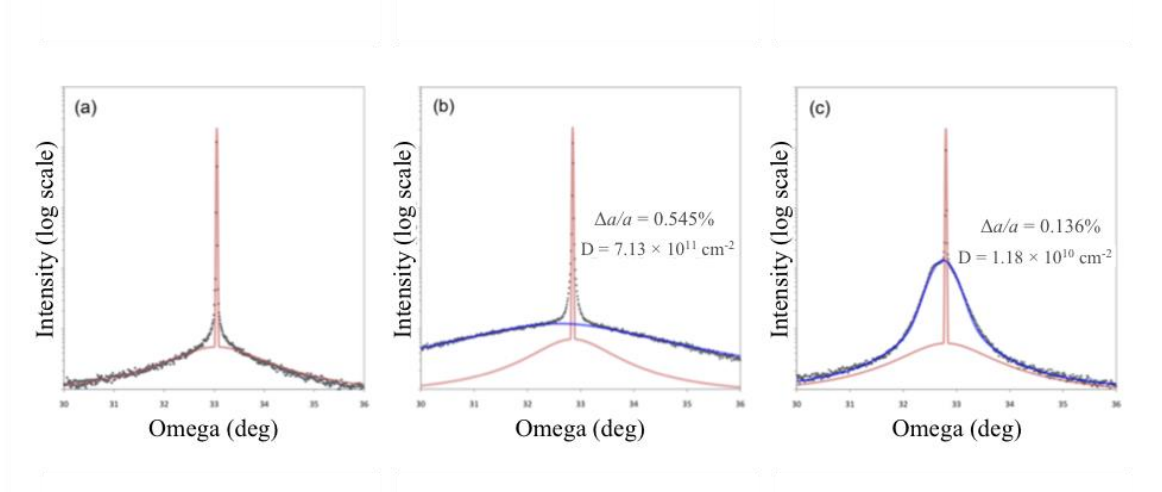


Figure 32. XRD Rocking Curves (logarithmic scale) measured about GaAs (400) plane for (a) bare GaAs substrate, (b) $ZnS_{0.1}Se_{0.9}$ (300 nm), and (c) $ZnS_{0.1}Se_{0.9}/Cr^{2+}$:ZnSe with 300:150 nm thickness ratio. In addition to the XRD data, calculated pseudo-Voigt fits for the peaks are displayed, which were obtained to aid in determining the dislocation density (D) and difference in lattice parameter ($\Delta a/a$) for each sample.

associated thin films of ZnS_xSe_{1-x} incur an identical tilted orientation during measurement, the determined values for the difference in lattice parameter between the substrate and corresponding layers are independent of sample tilt.

For optoelectronic applications, epitaxial growth of each layer of a multilayered thin film structure is supposedly desired to achieve the electronic and optical properties necessary for successful integration into an effective lasing device. However, achieving single crystal films of ZnSe-based materials above the critical thickness on GaAs via PLD poses a significant challenge. Considering that the concept structure in Figure 1 suggests ZnSe-based waveguiding layers surrounding the active region, these layers would need to approach a minimum of ~2 μm in individual layer thickness in order to provide effective optical confinement of the mid-IR emission of the Cr^{2+}:ZnSe active layer. As an alternate approach to a structure consisting of single crystal thin film layers (each multiple microns in thickness), a multilayered electroluminescent structure composed of polycrystalline layers of optimized crystal quality could potentially be realized.

5.6 Summary of Results

In efforts to successfully deposit epitaxial films of pulsed-laser-deposited ZnS_xSe_{1-x} on (100) GaAs substrates, sulfur content (x=0.02, 0.06, 0.10) and deposition temperature (400°C, 425°C, 450C) were varied to investigate the effects of these growth parameters on the crystallinity of the resulting thin films. Analysis of XRD 2θ glancing angle scans reveal most combinations of the two varied parameters to yield polycrystalline films, but 3 specific combinations (x=0.02/450°C, x=0.06/450°C, x=0.10, 425°C) resulted in XRD data indicative of epitaxy. Subsequent XRD rocking curves on the films displaying epitaxy

showed variable shifts in the film peak relative to the (400) GaAs substrate peak as sulfur content and deposition temperature were varied.

The smallest average difference between lattice parameter of film and substrate was measured to be $\Delta a/a$=0.017% and was obtained for the $ZnS_{0.02}Se_{0.98}$ (x=0.02) sample deposited at a temperature of 450^{o}C, which was an unexpected result considering the well-established lattice matching properties of $ZnS_{0.06}Se_{0.94}$ (x=0.06) grown atop GaAs. Analysis of the rocking curve FWHM of the (400) GaAs growth peak reveals the sample with the lowest average dislocation density of D=2.87x10^{10} cm^{-2} to be the $ZnS_{0.06}Se_{0.94}$ (x=0.06) film deposited at a temperature of 450^{o}C. The overall rocking curve widths of these samples are much broader than most epitaxially-grown single crystal thin films reported in the literature, and the measured dislocation densities and differences between lattice parameter of film and substrate were observed to increase with increasing film thickness of the illuminated region of the x-ray spot for a common sample. These characteristics are presumed to be consistent with epitaxially-oriented, polycrystalline structures, and are suggestive of varying degrees of relaxation as a function of film thickness and possible non-uniform distribution of sulfur atoms throughout the film structure during growth. This deviation from single crystal growth could be due to many factors, including excessively high laser fluence, high surface roughness of the GaAs substrate after etching, stacking faults cause by interaction of S at the GaAs interface, and/or shallow Ga-diffusion into the ZnS_xSe_{1-x} layer during deposition [74].

In order to improve the crystalline quality of the ZnSSe layer, a subsequent study was conducted on the effects of the presence of a Cr^{2+}:ZnSe interfacial layer of varying thicknesses on multilayered thin film structures consisting of a 300 nm $ZnS_{0.1}Se_{0.9}$ layer,

(100) n-GaAs substrates, and Ni contacts. XRD analysis was performed to determine crystal quality and phase composition of all samples. While the $ZnS_{0.1}Se_{0.9}$ sample with no Cr^{2+}:ZnSe interfacial layer displayed prominent polycrystalline diffraction features, an identical structure with a 150 nm Cr^{2+}:ZnSe layer added at the GaAs interface exhibited epitaxial features in the XRD data. As the thickness of the Cr^{2+}:ZnSe layer was increased, diffraction peaks corresponding to a polycrystalline configuration emerged and became more pronounced with increasing thickness. However, all samples remained highly textured in the (400) GaAs growth direction.

Dislocation densities along the primary growth direction in structure #1 and structure #2 were measured to be 7.13×10^{11} cm^{-2} and 1.18×10^{10} cm^{-2}, respectively. Not only did the addition of the 150 nm Cr^{2+}:ZnSe layer prove to be a critical component in determining the growth regime of the ZnS_xSe_{1-x} film, but the dislocation density measured from structure #2 was the lowest observed among all deposited samples in both studies, showing a vast improvement in crystal quality of the ZnS_xSe_{1-x} film, even though the structure was over 1.5 times the thickness of the films deposited in the first study. While this research is the first instance of ZnS_xSe_{1-x} being grown by means of PLD, even thicker growth of this material (or the ZnMgSSe quaternary alloy) is necessary for effective waveguiding implementation into a multilayered mid-IR lasing device. However, an alternate multilayered structure incorporating a thin ZnSe-based layer at the GaAs interface and highly-oriented polycrystalline ZnS_xSe_{1-x} layers (with integration of appropriate dopants) for achieving mid-IR electroluminescence is a promising system for future investigation.

CHAPTER 6

ELECTRICAL PROPERTIES OF ZnSe-BASED MULTILAYER STRUCTURES

6.1 Introduction

Understanding the phenomena that govern the electrical properties of our ZnSe-based multilayer structures is essential for achieving our goal of an electroluminescent device. As seen in Chapter 5, the PLD-grown films exhibit a substantial concentration of extended defects that will inevitably affect their electrical transport characteristics. Even the epitaxially-oriented films have large dislocation densities, and polycrystalline films are the norm above a critical thickness of 100-220 nm. The potential impact of grain boundaries must therefore be considered in the electrical properties. Moreover, it is also necessary to take into account the effect of ohmic and/or rectifying junctions at the various metal/semiconductor and semiconductor/semiconductor interfaces in our structures. These junctions may feature localized trap states that may need to be mitigated to achieve acceptable resistivities for electrical excitation. In order to study these effects, several multilayered thin film structures were produced and their electrical properties were correlated with sample characteristics, including thickness and crystal structure of the primary layers.

6.2 Structures Designed for Electrical Studies

A series of multilayered samples with the architecture shown in Fig. 33 were deposited for a study to relate the crystallographic and electrical properties of the samples. The main parameter varied in these thin film structures was the thickness *t* of the Cr^{2+}:ZnSe layer as listed in Table 2, which is reproduced here from section 5.4 for ease of reference.

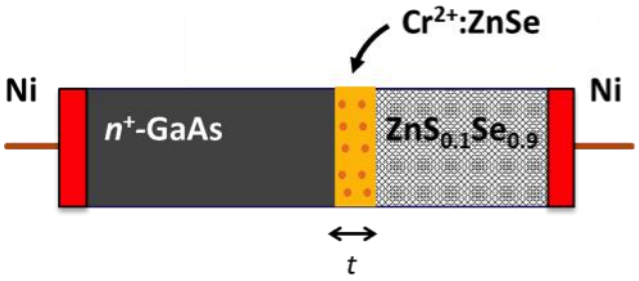


Figure 33. Layout of thin film structures designed for electrical characterization. The structure allows evaluation of the resistivity of the Cr^{2+}:ZnSe and ZnSSe layers as well as interfaces.

Table 2. Material Layer Thicknesses of Deposited Thin Film Structures

Structure	Thickness of $ZnS_{0.1}Se_{0.9}$ Layer (nm)	Thickness (*t*) of Cr^{2+}:ZnSe Interfacial Layer (nm)	Substrate
1	300	0 (no Cr^{2+}:ZnSe layer)	n-GaAs
2	300	150	n-GaAs
3	300	300	n-GaAs
4	300	450	n-GaAs
5	300	600	n-GaAs

6.3 General Electrical Characteristics of Designed Samples

For reference purposes, a primary structure of interest among those shown in Table 2 is structure #1, which contains no Cr^{2+}:ZnSe layer (*t*=0). This structure possesses the most

prevalent polycrystalline features as observed in the XRD data. As discussed in Chapter 5, the presence of sulfur atoms at the ZnSSe/GaAs interface leads to a large density of structural defects resulting in a polycrystalline ZnSSe film.

The impedance data displayed in Figure 34 for this reference structure allows identification of the most relevant processes that determine the electrical processes in this series. Figure 34a shows impedance arcs for an as-deposited sample while Figure 34b shows data for the same sample after annealing in forming gas. Considering first the as-deposited sample (Figure 34a), it is clear that the impedance of the structure is dominated by a large resistance arc of ~200 Ω (at zero bias) shown in the Nyquist plots in the low frequency regime. One also clearly notices the asymmetric behavior of this large arc as a bias voltage is applied to the sample. For positive polarity, the resistance of the large arc increases with increasing applied bias, which is the typical behavior of a Schottky junction under reverse bias. We can ascribe this arc to a Schottky-like junction at the interface between the $ZnS_{0.1}Se_{0.9}$ layer and the n^+-GaAs substrate, which would indeed be under reserve bias for positive polarity applied to the top Ni contact, assuming the presence of surface states. This $ZnS_{0.1}Se_{0.9}/n^+$-GaAs junction is in forward bias for negative polarity, and therefore would have negligible forward resistance. The decrease in resistance observed in the arc for negative polarity applied voltage is most likely due to the $ZnS_{0.1}Se_{0.9}$/Ni junction. This junction is either a low-barrier Schottky that leaks under reverse bias or features an accumulation layer with Fermi level pinned to interface states.

Additional arcs are visible in the Nyquist plots of Figure 34a in the high frequency regime with characteristic resistances below ~50 Ω. These high-frequency arcs are likely to contain useful information about the electrical properties of the interior of

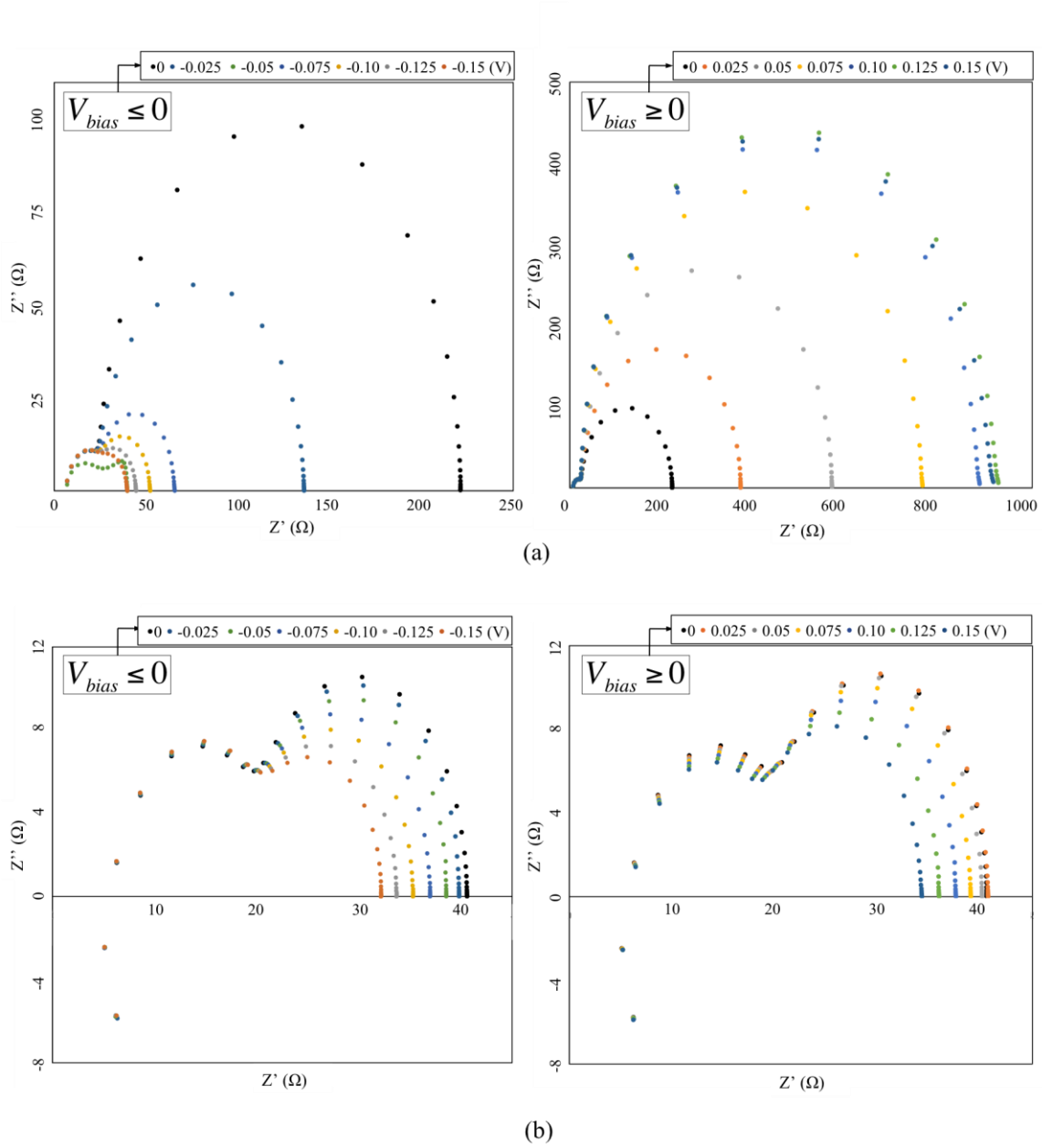


Figure 34. Nyquist Impedance data for structure #1 (a) as-deposited and (b) after annealing in forming gas under negative (left) and positive (right) applied bias voltages showing 2 arcs displaying different variations with applied voltage

the thin films in the structure, but their quantitative analysis is hampered by the dominance of the large arcs with hundreds of Ohms that are associated with interface phenomena. The presence of these large arcs underscores the importance of appropriate thermal treatments

to improve interface quality and passivate interface states. Figure 34b shows impedance arcs for the same sample of structure #1 after annealing in forming gas. The Nyquist plots now clearly show the arcs with resistance below ~50 Ω that were obscured by the interface arcs that dominated the as-deposited data. Remarkably, the impedance data is now essentially symmetric with respect to polarity reversal. Since the interface junctions in structure #1 are fundamentally asymmetric ($ZnS_{0.1}Se_{0.9}/n^{+}$-GaAs vs. $ZnS_{0.1}Se_{0.9}$/Ni), the symmetry of the impedance data with respect to polarity strongly suggests that we are now probing conductivity processes of the interior of the $ZnS_{0.1}Se_{0.9}$ layer. Turning to the details of the two arcs seen in Figure 34b, the behavior of the low frequency arc shows a decrease in resistance with applied voltage in both bias polarities, while the high frequency arc is independent of applied voltage in both polarities. In what follows, we explain how we can ascribe these two distinct arcs to different conduction processes in the interior of the ZnSSe film.

<u>High frequency arc</u>: *Grain interior conductivity in the polycrystalline ZnSSe layer*

The impedance arcs observed in Figure 34b are well described by the equivalent circuit model illustrated in Figure 35. Two parallel RC circuits in series and an additional series resistance R_S (attributed to the residual ohmic resistance of the sputtered contacts) provide an excellent fit to the experimental data as shown in Figure 36.

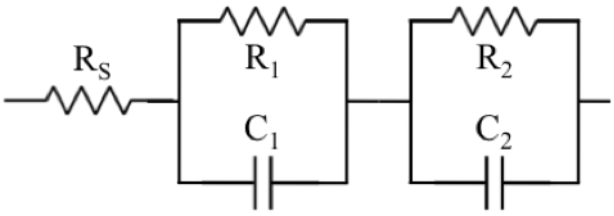


Figure 35. Equivalent circuit model of annealed structure #1 used to extract values of resistance, capacitance, and relaxation frequency for various processes in the ZnSSe layer

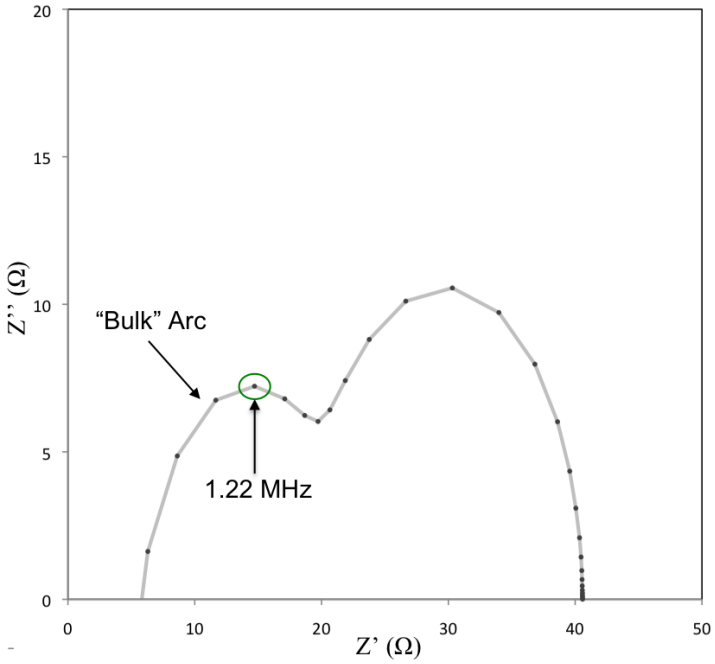


Figure 36. Nyquist plot displaying postanneal impedance data of structure #1 showing two arcs that can be associated with distinct conduction processes in the interior of the $ZnS_{0.1}Se_{0.9}$ layer. The relaxation frequency of the high-frequency arc is ~1.22 MHz as indicated.

The relaxation frequency of the high-frequency arc is measured to be 1.22 MHz, with a resistance R_1 = 13 Ω and a capacitance C_1 = 10 nF. These measured values are consistent with the electrical characteristics of a $ZnS_{0.1}Se_{0.9}$ film of 300 nm. Using the geometric capacitance of the $ZnS_{0.1}Se_{0.9}$ layer as a rough approximate model for C_1, one may write:

$$C = \varepsilon \frac{A}{d} \tag{44}$$

$$\tau = RC \tag{45}$$

$$f_C = \frac{1}{2\pi\tau} = \frac{d}{2\pi\varepsilon RA} \tag{46}$$

where $A = 2.5 \times 10^{-5}$ m^2, $d = 300 \times 10^{-9}$ m, and $\varepsilon = 8.87\varepsilon_0$ [61] are the parameters of the $ZnS_{0.1}Se_{0.9}$ layer. Using the measured R_1 and C_1 indicated above, the resulting time

constant was found to be 1.31×10^{-7} seconds, leading to a characteristic relaxation frequency of 1.22 MHz, which is in excellent agreement with the measured relaxation frequency of the high-frequency arc. This agreement, coupled with the fact that the high-frequency arc is voltage-independent, gives confidence in the designation of this arc as that of conduction through the "bulk" of the $ZnS_{0.1}Se_{0.9}$ film. Evidently, according to XRD analysis, the $ZnS_{0.1}Se_{0.9}$ film in this structure is not a single crystal. Therefore, the capacitance C_1 cannot be attributed to the simple geometric capacitance of a parallel plate capacitor. Likewise, the resistance R_1 is not the resistance of a single crystal $ZnS_{0.1}Se_{0.9}$ layer. The parallel $R_1//C_1$ circuit must therefore be interpreted as the equivalent circuit of the association of numerous $R_{gi}//C_{gi}$ circuits, with R_{gi} and C_{gi} representing the resistance and capacitance of each individual $ZnS_{0.1}Se_{0.9}$ grain. Determination of R_{gi} and C_{gi} from the measured values of R_1 and C_1 would require a detailed model of the microstructure of the layer.

Using the considerations above, the resistivity of the $ZnS_{0.1}Se_{0.9}$ material itself is estimated to be 1.95×10^{5} Ω•cm, which is consistent with an unintentionally lightly doped *n*-type material as intended in the structure fabrication.

Low frequency arc: *Tunneling-based conductivity in Schottky-like barriers at grain boundaries in the polycrystalline ZnSSe layer*

The low-frequency arc in Figure 34b is clearly voltage dependent. Greater detail is seen in Figure 37. Since its resistance decreases with applied voltage in both polarities, the arc behavior is most likely due to leakage current in double Schottky-like barriers at grain boundaries within the ZnSSe polycrystalline film. Figure 38 shows the expected band diagram at the grain boundary regions. When under an applied voltage of a given polarity,

approximately half of the barriers will be in forward bias with the other half in reverse. The barriers in forward bias have little impedance. The barriers in reverse, on the other hand, pose measurable resistance to the passage of current, particularly under low voltage. However, these barriers are unable to hold against the applied voltages, and their resistance decreases as the applied voltage is increased, leading to a non-ohmic behavior that is characteristic of varistor devices, which are actually designed on these principles based on polycrystalline materials. Therefore, the voltage-dependent, low-frequency arc represents the collective impedance contribution from grain boundaries within the ZnSSe layer [70].

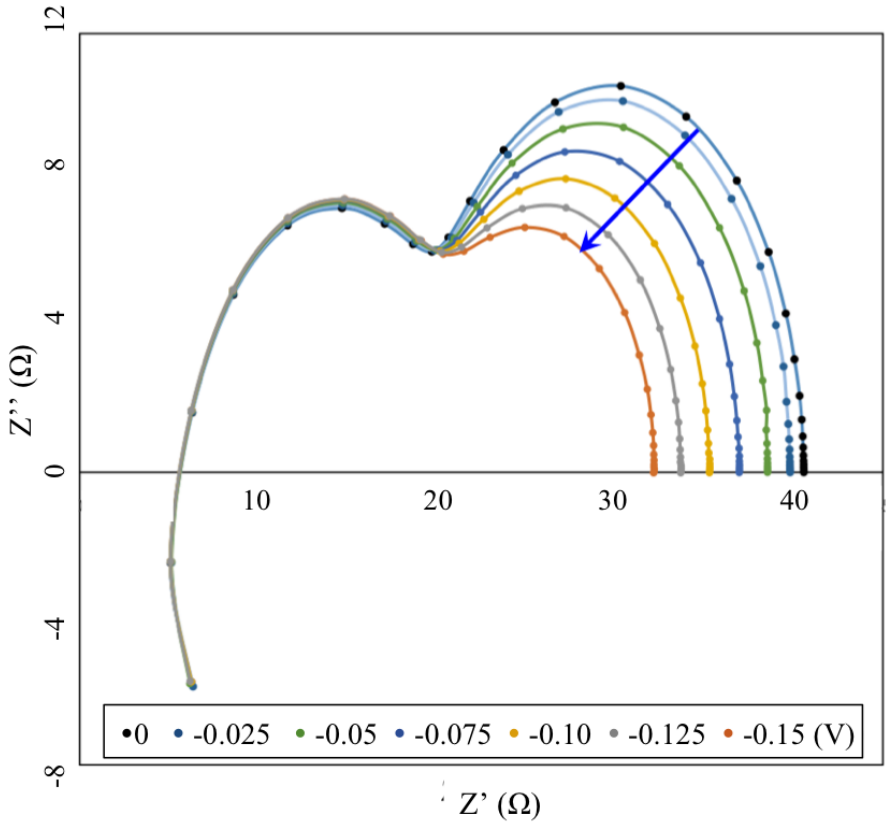


Fig. 37. Impedance data for the annealed ZnSSe film showing decreasing resistance of the low-frequency arc with increasing bias. This behavior can be attributed to leakage currents in a Schottky-like barrier under reverse bias at the grain boundaries of a polycrystalline material.

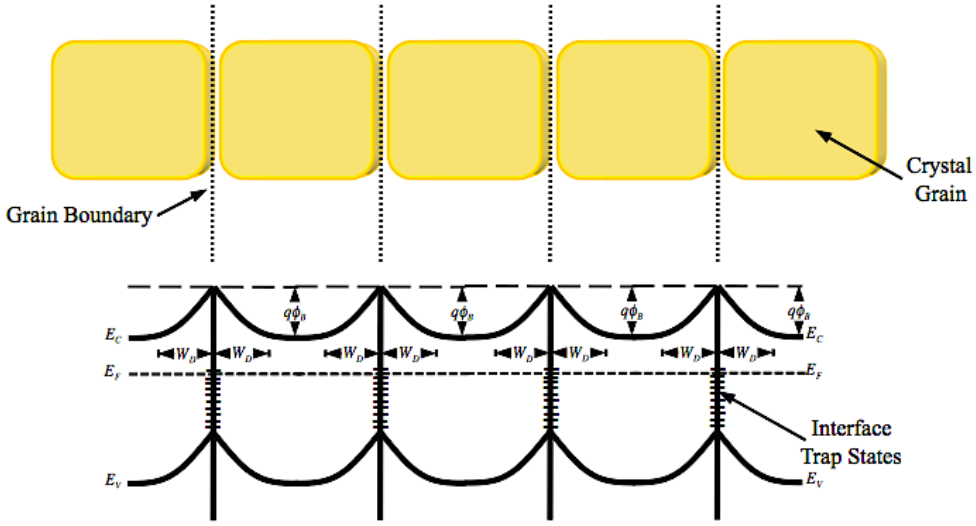


Figure. 38. Expected double Schottky-like band edge profile at grain boundaries in the ZnSSe film. Increasing applied voltages lead to reducing resistances due to growing leakage currents through potential barriers.

This interpretation is consistent with the current-voltage (I-V) characteristics of the structure as seen in Figure 39. The I-V is approximately symmetric with respect to the polarity of the applied bias voltage. This again indicates that the Schottky-like barriers formed at grain boundaries, which to a first approximation we assume to be randomly oriented, play an important role in governing current flow, which will be discussed later in the chapter. The symmetric behavior observed in the current-voltage data for the low frequency arc supports the idea that this arc arises from multiple, symmetric double-Schottky potential barriers created by the array of grain boundaries present across the structure. Furthermore, unlike any other structure produced in this study, the I-V data calculated from the low frequency arc for structure #1 shows a very close fit to a theoretical tunneling model (discussed in detail in the following sections) for all values of applied voltage up to 0.5 V, which suggests carrier tunneling to be the dominant current flow process through the ZnSSe grain boundaries for all bias voltages applied within this

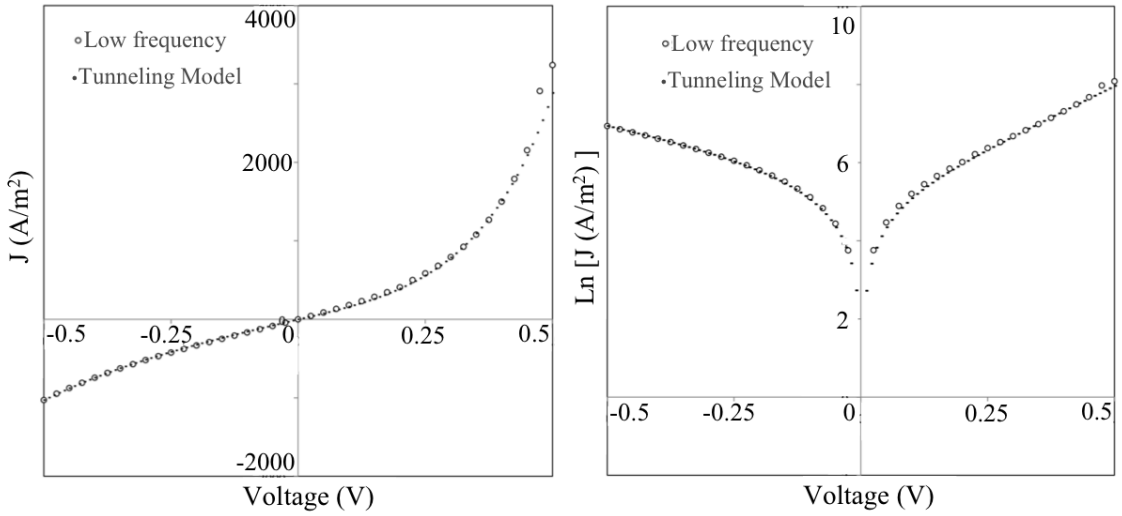


Figure 39. Current density versus voltage data for the low frequency arc in the ZnSSe/GaAs structure plotted along with corresponding tunneling model fits.

range, perhaps due to a larger role of defect-assisted tunneling [57] relative to the other structures, considering the high relative values of dislocation densities associated with structure #1.

6.4 Electrical Characteristics of Structures Containing a Cr^{2+}:ZnSe Layer

Having identified the basic underlying electrical transport phenomena in the reference sample of structure #1, we turn now to the analysis of samples containing a Cr^{2+}:ZnSe layer (structures #2-5). In all subsequent discussions, we focus on samples that were annealed in forming gas to reduce the interface resistances as demonstrated in the analysis of the reference structure #1.

6.4.1 The Varistor Behavior of the Cr^{2+}:ZnSe Layers and their Polycrystalline Character

Figure 40 shows the postanneal current density versus applied DC bias voltage for all

structures listed in Table 2. In all measurements, the reference electrode was in contact with the top side ($ZnS_{0.1}Se_{0.9}$ top, GaAs bottom) of each structure. The ohmic response of the GaAs substrate is also shown for reference. All samples exhibit non-ohmic behavior with the I-V curves approximately symmetric with respect to polarity reversal. In general, all structures show decreasing resistivity with increased applied voltage in both polarities. This is the overall behavior observed in varistor systems and suggests that grain boundary resistances between internal crystallite grains of the Cr^{2+}:ZnSe layer play an important role in the electrical properties. The data does reveal some level of asymmetry in the I-V curves (with higher resistances for negative polarity) that suggests the additional presence of at least one interface junction with rectifying properties. The possible origin of this asymmetry will be discussed later in this chapter. For the time being, we focus on the overall varistor behavior of the structures.

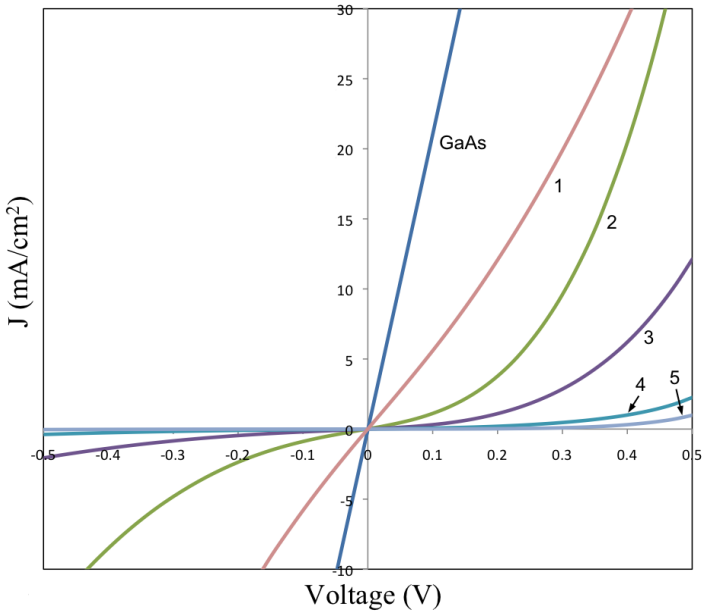


Figure 40. Current density versus applied DC bias voltage from -0.5 V to +0.5 V displayed for all reference structures (data obtained after annealing process)

Figure 41 complements the I-V curves of Figure 40, showing the impedance data for structures #2-5 under zero bias. The Nyquist plots show that at low voltage, all structures are dominated by a single impedance arc whose radius scales with the thickness of the Cr^{2+}:ZnSe layer, as expected. For all Cr^{2+}:ZnSe thicknesses, the arc observed at zero bias shows decreasing resistance when voltages of both polarities are applied, as seen in Figure 42 for the case of t = 450 nm (structure #4). This is of course consistent with the I-V curves shown in Figure 40, and once again the asymmetry with respect to polarity reversal that overlaid on the $R \propto 1/V$ general behavior is observed.

The overall decrease in resistance for both polarities with increasing voltage mirrors the behavior of the voltage-dependent arc seen in the reference sample with t = 0. This is the signature behavior of a varistor system with the largest source of resistance provided by double Schottky-like barriers at internal grain boundaries of a polycrystalline Cr^{2+}:ZnSe layer. This scenario of grain-boundary dominated electrical properties is supported by the crystalline configuration determined by XRD analysis of our PLD-grown structures. As seen in Figure 43, reflections for the (111), (200), and (220) families of crystal planes of the Zn(S)Se system are observed in the glancing angle 2θ XRD patterns. This indicates the polycrystalline nature of the Cr^{2+}:ZnSe layer, the ZnSSe layer, or most likely both materials, in structures #3-5. Since the XRD intensities are dominated by the Cr^{2+}:ZnSe layer in structure #5 (Cr^{2+}:ZnSe, 600 nm; ZnSSe, 300 nm), and the corresponding XRD pattern is unequivocally polycrystalline, it is safe to conclude that structures #3-5 contain polycrystalline Cr^{2+}:ZnSe layers. This conclusion is also supported by the fact that structures #3-5 contain Cr^{2+}:ZnSe above the critical thickness for epitaxy.

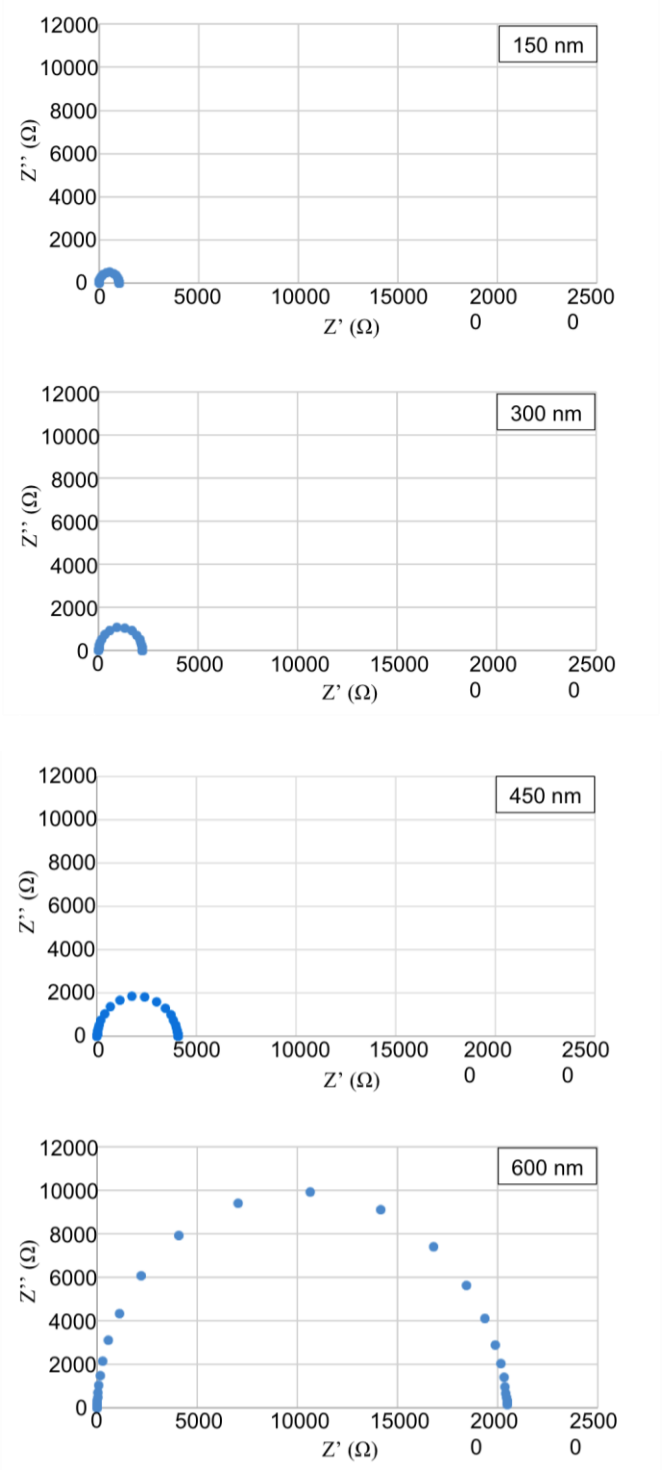


Figure 41. Impedance as a function of Cr^{2+}:ZnSe layer thickness under zero bias. Data obtained for structures #2-5. The Nyquist plots show that low voltage impedance is dominated by a single impedance arc.

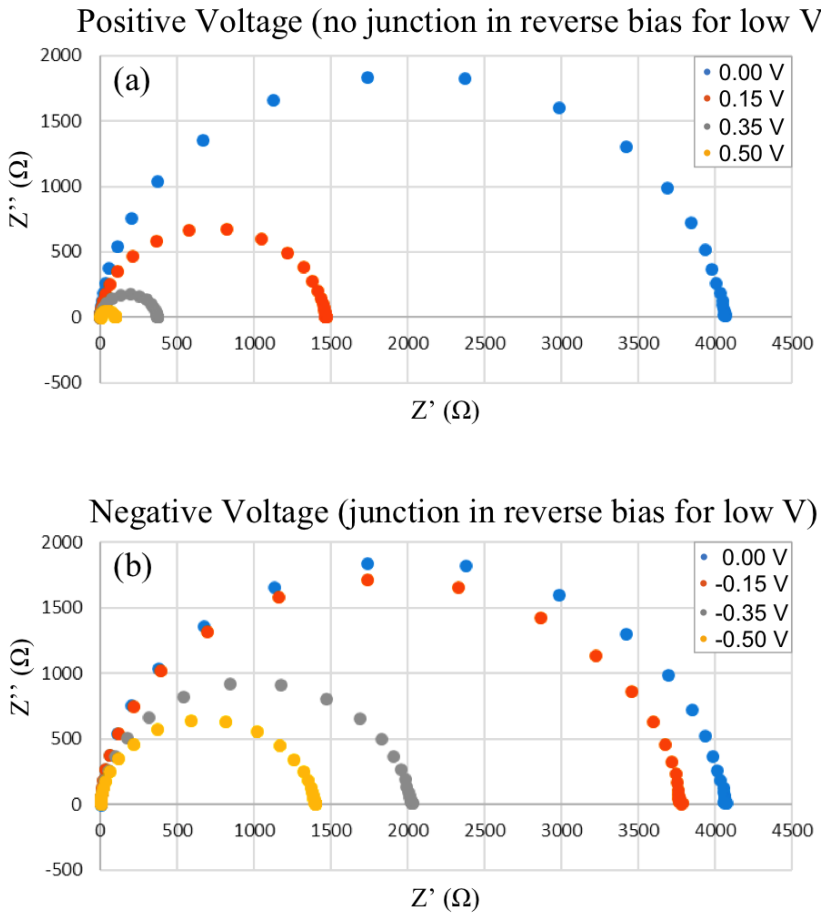


Figure 42. Plots showing effects of (a) positive and (b) negative applied voltage on the impedance of the structure containing a Cr^{2+}:ZnSe layer with t = 450 nm (structure #4)

The XRD measurements shown in Figure 43 allow an assessment how the number of grain boundaries varies in these various structures. The patterns in Figure 43 reveal that as the thickness of the Cr^{2+}:ZnSe layer is increased, the intensities of the reflections that are "non-epitaxial" with respect to the substrate increase relative to the intensity of the "epitaxial" reflection. The increase in the relative peak heights of the non-epitaxial peaks indicates a trend away from epitaxial orientation and consequent increase in number of

grain boundaries due to crystal misalignment of adjacent grains. Relative peak intensities were determined from the XRD patterns displayed in Figure 43 and are listed in Table 3.

Most of the diffraction peaks observed in the XRD data in Figure 43 are found at values of 2θ that lie somewhere in between the predicted values for ZnSe and ZnS for a common crystal plane, so these peaks are being referred to here as the Zn(S)Se group rather than by the independent diffraction peak locations of ZnSe and ZnS. The peaks P_1, P_2, and P_3 referenced in Figure 43 and Table 3 refer to the Zn(S)Se (111), Zn(S)Se (200), and Zn(S)Se (220) growth peaks, respectively, and the intensities of these diffraction peaks were all measured relative to the Zn(S)Se (311) primary growth peak (P_{ref}) as observed in the XRD glancing angle 2θ data. While the P_1 Zn(S)Se (111) and P_2 Zn(S)Se (200) peaks were observed to increase for samples #3-5 as a function of thickness of the Cr^{2+}:ZnSe layer, the P_3 Zn(S)Se (220) growth peak showed a less significant increase in relative height. The increase of relative peak height of the non-epitaxial growth peaks as a function of increasing thickness of the Cr^{2+}:ZnSe layer indicate an increase in polycrystalline features such as number of crystallites, grain boundaries and mosaicity within the layer.

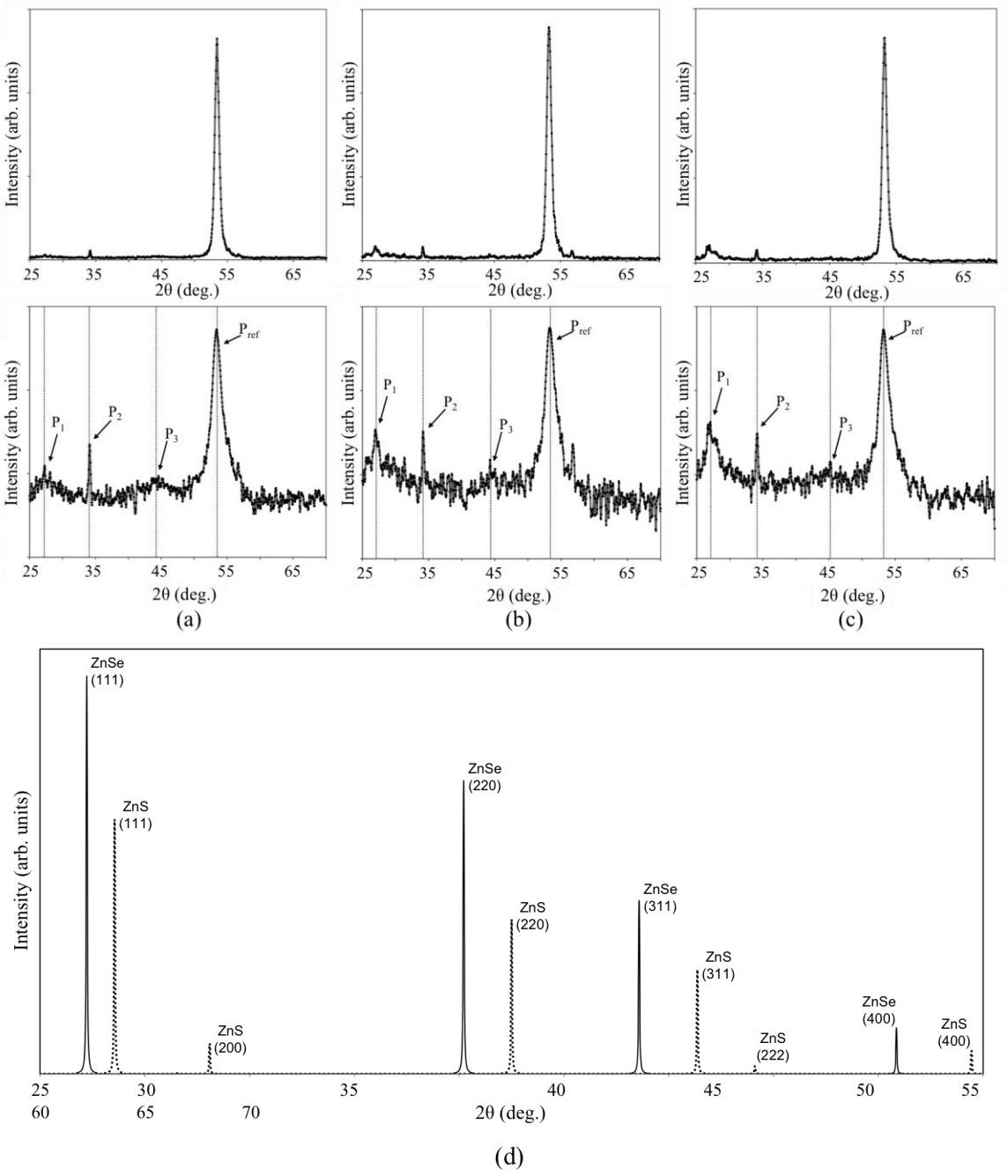


Figure 43. XRD Glancing Angle 2θ Scans of polycrystalline thin film structures showing relative heights of various observed diffraction peaks displayed in linear (top row) and logarithmic scale (middle row) for (a) sample #3, (b) sample #4, and (c) sample #5, along with (d) standard diffraction patterns for ZnSe (cubic) and ZnS (cubic) for comparison

Table 3. XRD Diffraction Peak Intensities measured relative to Primary (311) Zn(S)Se Growth Peak in Deposited Thin Film Structures

Sample	P_1 / P_{ref}	P_2 / P_{ref}	P_3 / P_{ref}
3	0.026	0.049	0.018
4	0.059	0.061	0.026
5	0.078	0.064	0.026

6.4.2 Analysis of the Grain Boundary Resistivity of the Cr^{2+}:ZnSe Layer

An essential characteristic of the grain boundary resistance that dominates the electrical behavior of the Cr^{2+}:ZnSe layer is the barrier height of the Schottky-like junctions at the boundaries. In order to extract experimental values for the effective heights of the potential barriers formed at these boundaries, the method described in section 4.3 was employed for the all structures, but only within a range of applied bias voltages corresponding to dominant current contributions of thermionic emission.

In all postanneal structures analyzed in this study, there appears to be two primary mechanisms driving current flow, one of which becomes dominant in certain voltage regimes. At low bias voltages (near 0 V), carrier tunneling appears to be the dominant process for charge transport. Conversely, thermionic emission dominates at high bias voltages (approaching 0.5 V) as the Fermi level is raised closer to the conduction band edge. These trends are observed by fitting theoretical models to the I-V data, using carrier tunneling or thermionic emission as the dominant processes of charge transport in the appropriate voltage regime. Theoretical values of the tunneling current density were calculated using the following expression [58]

$$J_t \sim A^{**} B e^{-q\phi_B / E_{00}} e^{qV / E_{00}} \qquad (47)$$

where

$$E_{00} = \frac{qh}{2}\sqrt{\frac{N_D}{\varepsilon_S m^*}} \tag{48}$$

where E_{00} is an energy constant of the material and is associated with the WKB expression for the transmission of the barrier [59]. For the theoretical model of the tunneling current, the relative permittivity of ZnSe (ε_S=9.1ε_0) and effective electron mass in the ZnSe system (m^*=0.17m_e) [60] were used in conjunction with barrier heights extracted from current-voltage data to formulate theoretical fits to the experimental values of current density versus voltage, using N_D and B as fitting parameters (where B is a parameter related to the temperature and Fermi level in the semiconductor).

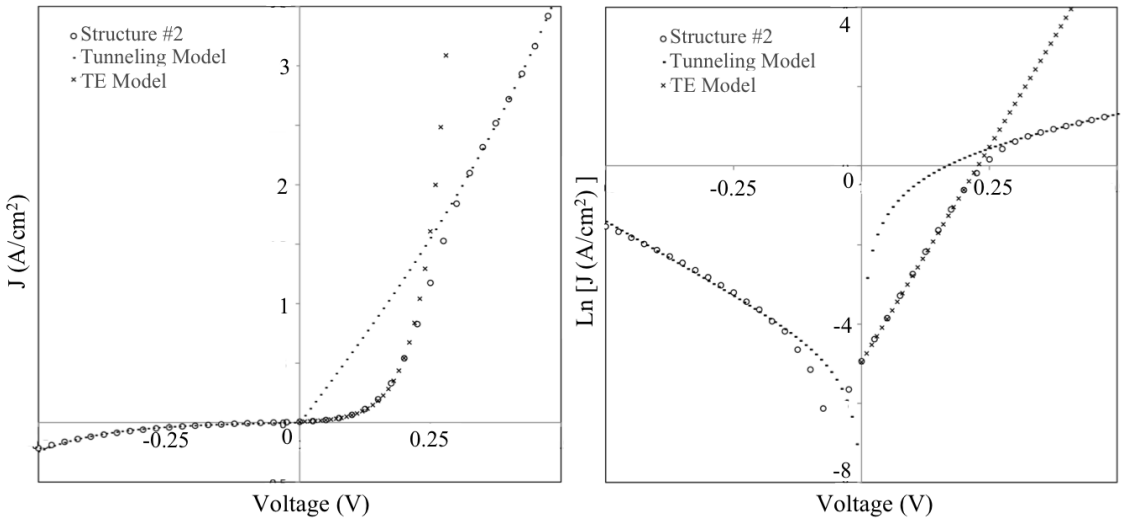


Figure 44. Plots of measured values of preanneal current density versus applied bias voltage for structure #2 (with accompanying log scale plots) plotted with theoretical fits to show transition between dominant transport processes of thermionic emission (TE) to carrier tunneling with increasing voltage, which is the opposite trend observed in the postanneal data

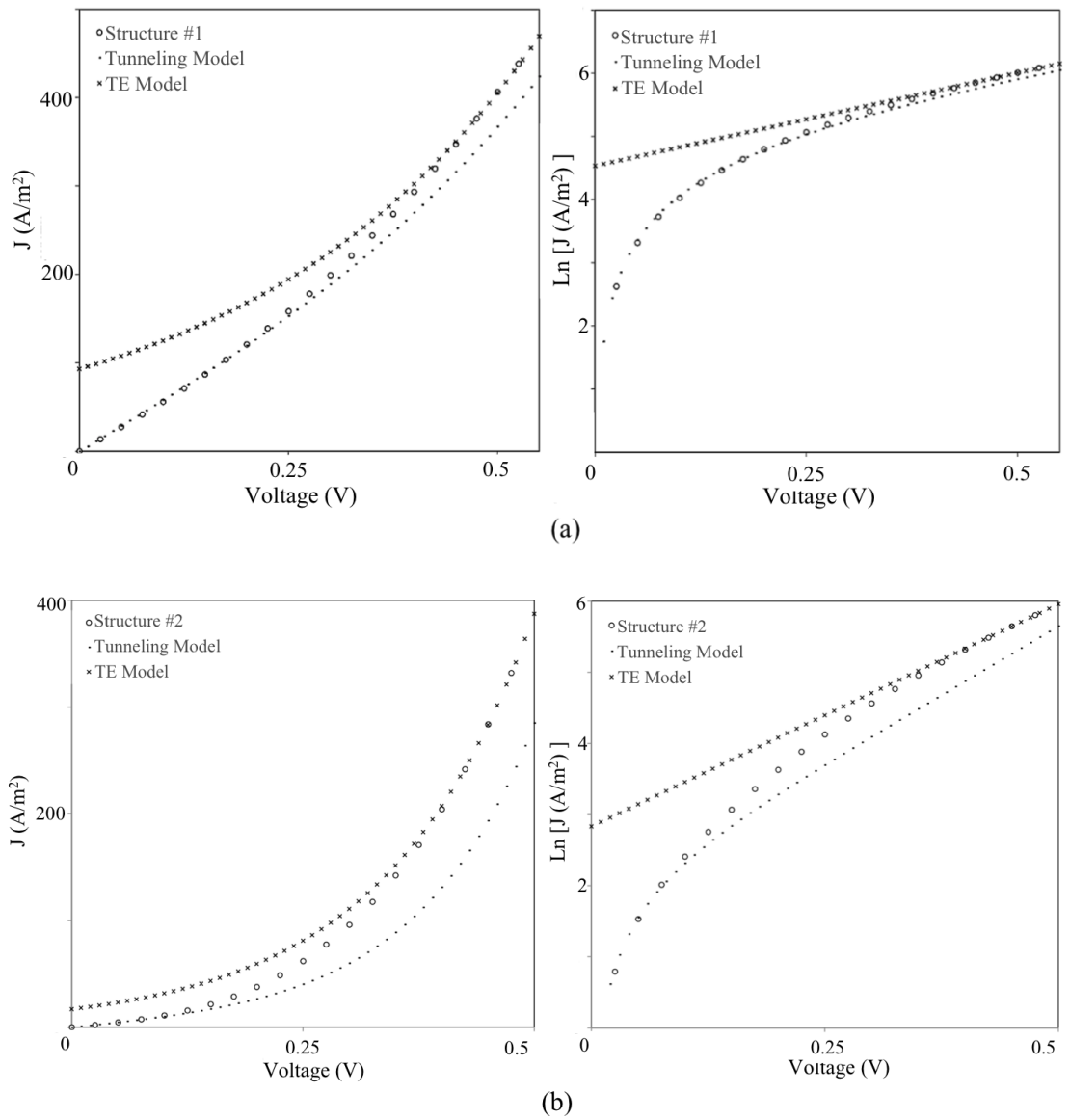


Figure 45. Linear and log scale plots of current density versus applied bias voltage for (a) structure #1 and (b) structure #2, showing the shift in the transition of the dominant current flow process of carrier tunneling to thermionic emission (TE) to increasing values of bias voltage as a function of sample polycrystallinity

The tunneling contribution to charge transport appears to be the dominant process for net current flow in all structures at low voltages except for preanneal current-voltage data of epitaxially-oriented structure #2, which indicates the opposite trend with a clear transition of the dominant charge transport process from thermionic emission at low voltages to tunneling at higher voltages (in the positive-bias regime). After annealing, the

dominant tunneling component in structure #2 appears to have shifted to lower voltages, while thermionic emission becomes dominant at higher voltages, as observed in all other postanneal structures. As the number of polycrystalline features increase throughout the structures (as observed in the XRD data), the transition of the dominant current flow process from tunneling to thermionic emission is observed to shift towards lower bias voltages. This is possibly due to a more pronounced narrowing of the double-Schottky barriers throughout structures with increased dislocation densities and polycrystalline features relative to structures displaying superior crystal quality.

Since all postanneal structures in this study display a closer fit to a thermionic emission model at voltages approaching 0.5 V, barrier height determination via the thermionic emission method is utilized in this voltage range. Recall from section 4.3 that by plotting the natural log of the current density versus applied bias voltage, the effective barrier height is extracted from the y-intercept of the extrapolated linear fit to the log-linear region (see Figures 46 & 47). Effective barrier heights determined from the current density versus bias voltage data are listed in Table 4, along with corresponding values for the (postanneal) specific contact resistance of the junctions which were calculated by [54,56]

$$R_C = \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0} \tag{49}$$

Equation 20 and equation 49 can be combined to yield

$$R_C = \frac{k}{qA^{**}T} e^{q\phi_B/kT} \tag{50}$$

Inserting material parameters and known constants into equation 50 gives a value for the specific contact resistance of the junction in units of $\Omega \cdot cm^2$. Dividing these values by the area of the contact (cm^2) gives a corresponding value of the resistance (Ω) contributed by

the respective junction. Since Equation 49 utilizes the partial derivative of the thermionic emission current density with respect to applied voltage, the calculated values of R_C are not expected to match the corresponding resistances of the Nyquist arcs with great accuracy at zero voltage, since tunneling appears to dominate over thermionic emission at low voltages (see Figure 45). This trend is found for all postanneal structures with varying degrees of prevalence of tunneling and thermionic emission at low and high voltages, respectively.

Effective barrier heights listed in Table 4 were determined using the values of total current density measured for the respective structures. Values of specific contact resistance calculated from thermionic emission theory were consistently lower than the measured resistances displayed in the impedance arcs at zero bias by a factor of ~4. This underestimation of the net resistance of the potential barriers associated with the collection of grain boundaries is likely due to using the expression for thermionic emission to derive equation 50 rather than the expression for carrier tunneling shown in equation 47. Determination of these values of contact resistance via the tunneling equation was not possible due to the ambiguity of the parameter B within our structures.

Table 4. Values of Effective Barrier Height and Contact Resistance calculated from Postanneal Current Density versus Applied Bias-Voltage Measurements on Deposited Thin Film Structures

Sample	Thickness of Cr^{2+}:ZnSe Layer (nm)	ϕ_B $(-V_{bias})$ (eV)	ϕ_B $(-V_{bias})$ (eV)	R_C / Area $(+V_{bias})$ (Ω)	R_C / Area $(-V_{bias})$ (Ω)
1	N/A	0.509	0.505	6.7	5.7
2	150	0.553	0.557	165.4	193.0
3	300	0.592	0.597	404.4	490.2
4	450	0.639	0.638	1043.1	1003.7
5	600	0.662	0.690	1642.2	4820.8

The values of grain boundary resistance inferred from R_C and the overall resistance of the Cr^{2+}:ZnSe allow the determination of an important figure of merit of the layer: the effective resistivity and how crystal quality of the structure may affect it. Table 5 displays relevant parameters and calculated values of effective resistivity for each layer present in the samples analyzed in this study. In order to extract values of resistance for the Cr^{2+}:ZnSe layers in structures #2-5, the independent values of resistivity for the GaAs substrate and 300 nm $ZnS_{0.1}Se_{0.9}$ layer (both with deposited Ni contacts) were calculated using the equivalent circuit model method applied to the GaAs sample and structure #1.

Resistivity values of 31 Ω•cm and 1.95×10^5 Ω•cm were calculated for the Ni/GaAs/Ni system and $ZnS_{0.1}Se_{0.9}$ layer, respectively. These values of resistivity, in conjunction with extracted values for the specific contact resistance for the Schottky junctions present in each sample, were applied to subsequent equivalent circuit models of samples #2-5 to isolate values of resistance solely contributed by the Cr^{2+}:ZnSe layers. These resistances were then used, along with relevant sample parameters, to calculate upper bounds to the effective resistivity (ρ*) of the Cr^{2+}:ZnSe layer.

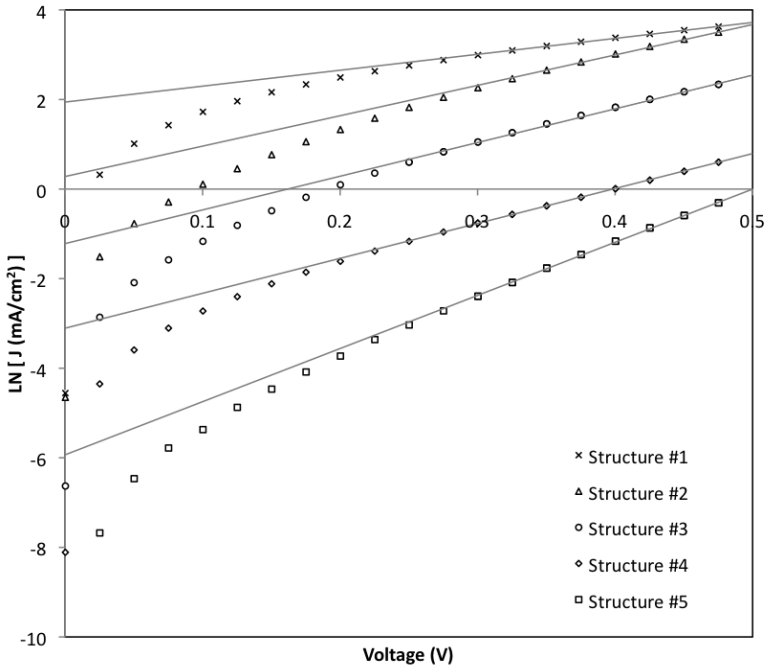


Figure 46. Postanneal data of the natural log of current density versus *positive* applied bias voltage used in effective barrier height determination for structures #1-5

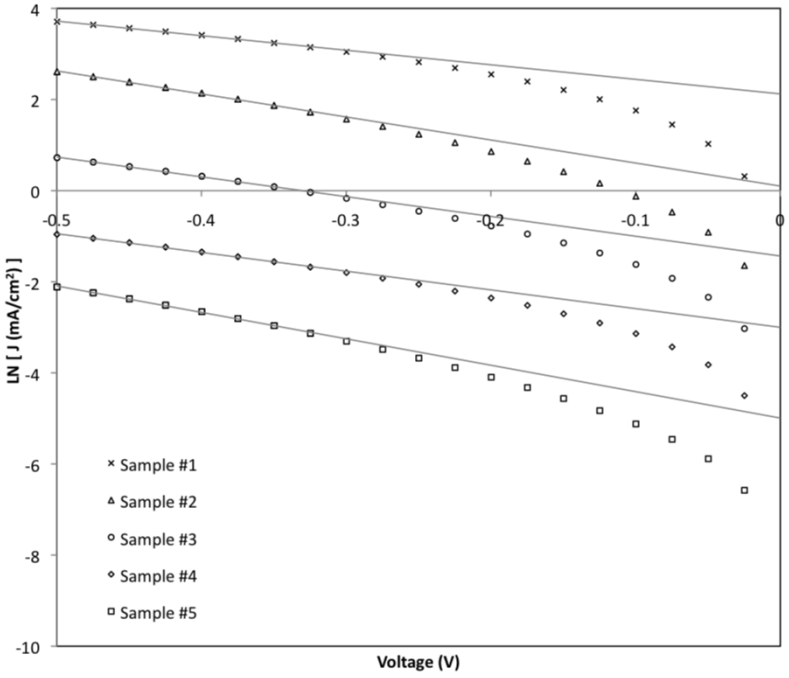


Figure 47. Postanneal data of the natural log of current density versus *negative* applied bias voltage used in effective barrier height determination for structures #1-5

Table 5. Electrical Properties of Deposited Thin Film Structures

Sample	Contact Area (cm^2)	R_{Total} (Ω)	$R_{Cr^{2+}:ZnSe}$ (Ω)	$\rho^*_{Cr^{2+}:ZnSe}$ (Ω•cm)
GaAs	0.55	2	N/A	N/A
1	0.45	13	N/A	N/A
2	0.12	1000	760	6.1×10^6
3	0.22	2200	1755	1.3×10^7
4	0.52	4070	3009	3.5×10^7
5	0.80	20483	18830	2.5×10^8

The observed increase in the effective resistivity of the Cr^{2+}:ZnSe layer can be attributed to an increase in the number of grain boundaries with increasing layer thickness as confirmed by the XRD analysis.

For dopant concentration characterization, a slightly different approach must be taken from the conventional capacitance-voltage method discussed in Chapter 4 due to the complex polycrystalline microstructure of these samples. Instead of using the relationship of the variation in total capacitance versus applied voltage, an approach utilizing the isolated capacitance of the grain boundaries must be taken. The equation relating the voltage-dependent nature of the grain boundary capacitance is given by [71]

$$\left(\frac{1}{C_{gb}}-\frac{1}{2C_{gb_0}}\right)^2=\frac{2p^2}{qk\varepsilon_0 N_D}\left(\phi_B+\frac{V}{p}\right) \tag{51}$$

where ϕ_B is the barrier height, V is the applied voltage, N_D is the dopant concentration, p is a normalization parameter dependent on the number of active barriers within the material, and C_{gb} and C_{gb0} represent the grain-boundary capacitance under applied voltage V and V=0, respectively.

6.4.3 Double Varistor Behavior of Epitaxially-oriented Cr^{2+}:ZnSe/$ZnS_{0.1}Se_{0.9}$ Structure

The varying degrees of crystallinity noted as a function of thickness in the structures discussed in Section 6.4.2 (structure #3-5) showed that the overall resistivity of the Cr^{2+}:ZnSe layer scales with the number of grain boundaries in the film. This is consistent with our varistor model where the observed current is governed by tunneling through the numerous grain boundary regions in the polycrystal. It is also interesting to consider the varistor behavior of structure #2, which contains a Cr^{2+}:ZnSe that is epitaxially-oriented with respect to the GaAs substrate. The Cr^{2+}:ZnSe layer in structure #2 has t = 150 nm, which is at or below the critical thickness for epitaxy of ZnSe on GaAs. Despite epitaxial orientation, this highly textured sample is unlikely to be a single crystal given the typical levels of mosaicity seen in PLD-grown films.

Nevertheless, the lower overall resistance of the Cr^{2+}:ZnSe varistor allows the observation of additional impedance features in the range of applied voltages accessed in our experiments. This is seen in Figure 48, which shows the impedance arcs for the 150-nm Cr^{2+}:ZnSe sample for applied voltages of both polarities. As was the case for the structures with thicker layers, the large varistor arc that dominates the impedance plane shows decreasing resistance with applied voltage. The behavior is approximately symmetric with respect to polarity reversal as also noted for the greater thicknesses. However, at sufficiently high applied voltages (V = +0.225 V, positive polarity; V = –0.475 V, negative polarity), a second arc manifests itself in the impedance plot. This second arc becomes particularly clear in the case of $V > 0$, shown magnified in the bottom region of Figure 48. Both arcs change with applied voltage, which rules out their origin in conduction processes of the grain interiors. Their characteristic magnitudes,

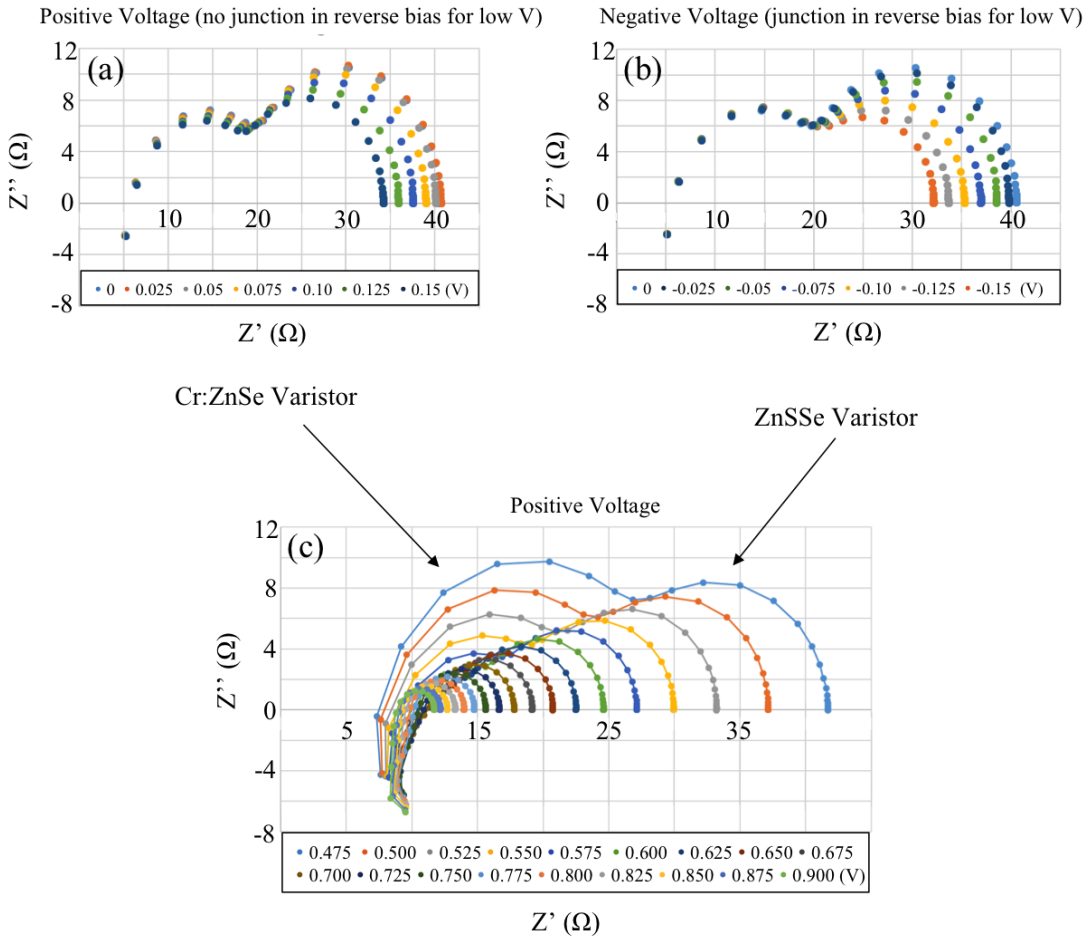


Figure 48. Impedance of structure #2 containing an epitaxially-oriented Cr^{2+}:ZnSe layer of 150-nm thickness under (a) positive and (b) negative polarities. Panel (c) shows the arcs obtained at higher voltages for positive applied voltage. Both arcs are clearly voltage dependent, with resistance decreasing with applied voltage, consistent with their assignment to the Cr^{2+}:ZnSe and ZnSSe varistors as indicated in the figure.

dependence of relaxation frequency, and a comparison with the ZnSSe (structure#1) impedance reveal that the low frequency arc, which is new arc to emerge, represents the ZnSSe varistor layer. As voltage increases, the resistance of the ZnSSe decreases as tunneling currents grow through the Schottky-like barriers in reverse in that layer. On the other hand, the high-frequency arc, which is also voltage-dependent, originates in the Cr^{2+}:ZnSe varistor. The high frequency of the Cr^{2+}:ZnSe varistor arc (in excess of 1 MHz)

is a result of the very low resistance and capacitance of this layer under high applied fields. As the applied voltage increases, the resistivity of both varistor layers becomes very small, leading to high currents in the overall structure.

6.4.4 Asymmetry of the Impedance Characteristics of the Cr^{2+}:ZnSe Layers

As alluded to in Section 6.4.1 and noted in Figures 40 and 42, all structures containing Cr^{2+}:ZnSe layers exhibit some level of asymmetry in the impedance with respect to polarity reversal. Since the varistor behavior is essentially associated with polycrystalline structures, whose grain boundaries are randomly oriented, the varistor scenario in the Cr^{2+}:ZnSe and ZnSSe layers cannot account for the observed impedance asymmetry. One must invoke the presence of at least one rectifying junction in these structures that is under reverse bias when the applied voltage has negative polarity (thereby increasing the resistance of the structure). Under forward bias (positive applied voltage in this case), the junction would pose low resistance resulting in smaller arcs in the Nyquist plots as is seen in Figure 42. The three interfaces indicated in Figure 49 (labeled *A*, *B*, and *C*) are in principle candidates for such a rectifying junction.

Interface *"A"* is an unlikely candidate because the n^+-GaAs/Cr^{2+}:ZnSe interface probably results in ohmic behavior after annealing and passivation of interface states. This is because the work function of the degenerate GaAs ($\leq$ 4.09 eV) is certainly less than the work function of Cr^{2+}:ZnSe (~5.0±0.5 eV), and the band offset in the conduction band of this interface ($\leq$ 300 meV), is not sufficient to create a Schottky barrier. Even in the improbable case that an interface state with appreciable concentration remains at interface

"*A*," leading to a Schottky junction, such a junction would be in forward bias when a negative voltage is applied to the structure, which cannot explain our results. Interface *"B"* is also unlikely to be source of rectification because no barrier was detected for negative applied voltages in samples with an identical interface (see Figure 34b). We therefore tentatively assign the rectifying behavior in the structures containing a Cr^{2+}:ZnSe to a "p-n junction-like feature" at interface *"C,"* as illustrated in Fig. 50. The fact that the Ni/$ZnS_{0.1}Se_{0.9}$ interface probed in Figure 34b show no rectification suggests that the work function of $ZnS_{0.1}Se_{0.9}$ is approximately equal or greater than the corresponding value for Ni (i.e., 5.2 eV). This places the Fermi level in the ZnSSe at least 5.2 eV below the vacuum level. This is consistent with the high resistivity of our ZnSSe layers (~10^5 Ω·cm). On the other hand, the high density of high-lying states associated with the Cr^{2+} dopant in ZnSe, suggests that the Fermi level in Cr^{2+}:ZnSe could be above the one for ZnSSe. If realized, these circumstances produce a junction that would be in reverse bias when an negative polarity is applied to the structures containing the Cr^{2+}:ZnSe, in qualitative agreement with the observed behavior of our samples.

Although plausible, this scenario needs to be verified by additional experiments. Adjustment of the Fermi level in ZnSSe by intentional *n*-type doping, correlated with impedance measurements would be one route to confirm or rule out this interpretation of rectification in these structures.

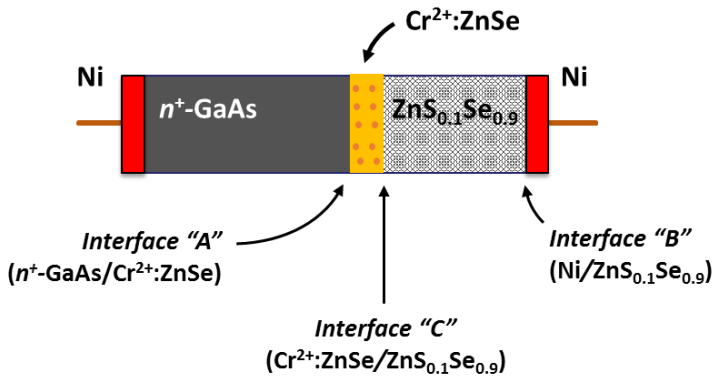


Figure 49. Schematic of the structures containing a Cr^{2+}:ZnSe layer and the candidate interfaces (labeled *A*, *B*, and *C*) for a junction providing current rectification under negative applied bias voltage.

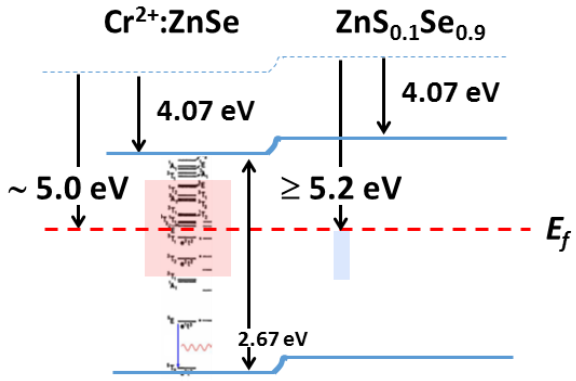


Figure 50. *p-n* junction-like interface posed to be present at Cr^{2+}:ZnSe/$ZnS_{0.1}Se_{0.9}$ heterojunction, likely providing current rectification under negative applied bias voltage

6.5 Summary of Results

A study was conducted on the effects of the presence of a Cr^{2+}:ZnSe layer of varying thicknesses on multilayered thin film structures incorporating a 300 nm $ZnS_{0.1}Se_{0.9}$ waveguiding layer, (100) n-GaAs substrates, and Ni contacts. XRD analysis was performed to determine crystal quality and phase composition of all samples. While the $ZnS_{0.1}Se_{0.9}$ sample with no Cr^{2+}:ZnSe layer at the GaAs interface displayed polycrystalline diffraction features, an identical structure but with a 150 nm Cr^{2+}:ZnSe layer added at the GaAs interface exhibited epitaxial features in the XRD data. As thickness of the Cr^{2+}:ZnSe layer was increased, extraneous diffraction peaks emerged and became more pronounced with increasing thickness. This increase in relative secondary peak height, along with an increasing value for calculated contact resistance, indicates an increase in grain boundaries in structures as a function of increasing thickness of the Cr^{2+}:ZnSe layer.

Following crystallographic analysis, metallic (Ni) contacts were deposited on both sides of all samples for electrical characterization. EIS was performed to determine the electrical properties of the structures before and after an annealing process in forming gas background at 300°C for 5 minutes. The annealing process provided significant increases in conductivity by lowering the various potential barriers formed at the Ni/$ZnS_{0.1}Se_{0.9}$ and GaAs/$ZnS_{0.1}Se_{0.9}$ (or GaAs/Cr^{2+}:ZnSe) Schottky junctions for all samples, allowing for effects from the interior grains and grain boundaries to be investigated. Current-voltage data of annealed structures shows the dominant current flow mechanism to be carrier tunneling at low bias voltages, and a transition towards thermionic emission as the dominant process occurs with increasing voltage. From effective barrier heights determined from current-voltage data, postannealed samples were found to show an

increase in effective barrier height and contact resistance due to collective grain boundary contributions with increasing thickness of the Cr^{2+}:ZnSe layer.

Equivalent circuit models were used to calculate values of resistivity for the various material layers incorporated throughout samples produced in this study using EIS data obtained after the annealing process. Using the voltage-independent impedance arc obtained at high frequencies, the resistivity of the 300 nm $ZnS_{0.1}Se_{0.9}$ layer was calculated to be 1.95×10^{5} Ω•cm. The calculated resistivity of the Cr^{2+}:ZnSe layer increased within the range $6.1\times10^{6} – 2.5\times10^{8}$ Ω•cm with increasing layer thickness, and the observed increase in resistivity is deemed to be due to the increase in the number of grain boundaries throughout the structures with increasing thickness. This hypothesis is supported by the increase in "non-epitaxial" growth peaks displayed in the XRD data as a function of increasing thickness.

The rectifying behavior still observed after annealing is proposed to be due to the presence of a p-n junction-like heterojunction at the Cr^{2+}:ZnSe/$ZnS_{0.1}Se_{0.9}$ interface. This study has proven valuable in verifying the need for implementing a ZnSe-based buffer layer at the GaAs interface to the proposed structure in Figure 1. Future directions include depositing the Cr^{2+}:ZnSe active layer between n-type and p-type $ZnS_{0.1}Se_{0.9}$ guiding layers, and deposition of a thin ZnSe buffer layer of appropriate thickness at the GaAs interface. Other next steps include performing Transmission Electron Microscopy on samples to characterize defect density and type, and performing luminescence measurements to test for dependence of mid-IR emission on crystal quality and grain boundary contributions.

CHAPTER 7

ELECTROLUMINESCENCE IN ZnSe-BASED THIN FILM STRUCTURES

7.1 Basic Structure and Crystallographic Characterization

As a preliminary milestone towards potential mid-IR electroluminescence in Cr^{2+}:ZnSe thin film structures, efforts were made to achieve visible emission from Cr^{2+}:ZnSe thin film structures under electrical excitation. The substrate chosen to be the deposition platform for a Cr^{2+}:ZnSe electroluminescent structure was composed of a thin layer of conductive indium tin oxide (ITO) on top of glass. The ITO/Glass substrates were selected over GaAs for this application due to high electrical conductivities of ITO thin films and high optical transmission in the spectral region of interest for potential mid-IR emission (see Figure 51). However, deposition of polycrystalline films of ZnSe was expected due to the large mismatch in lattice parameter between cubic ZnSe (5.668 Å) and cubic ITO (which is typically ~10 Å but varies with the composition of Sn in the alloy) [63].

Thin films (~3-4 μm) of Cr^{2+}:ZnSe were deposited onto ITO/Glass substrates via PLD using a Cr^{2+}:ZnSe ablation target produced in-house by mixing appropriate masses of ZnSe powder and CrSe powders (both 99.999% purity) to achieve a nominal Cr concentration of ~1.2×10^{20} cm^{-3}. In order to utilize the conductive ITO layer beneath

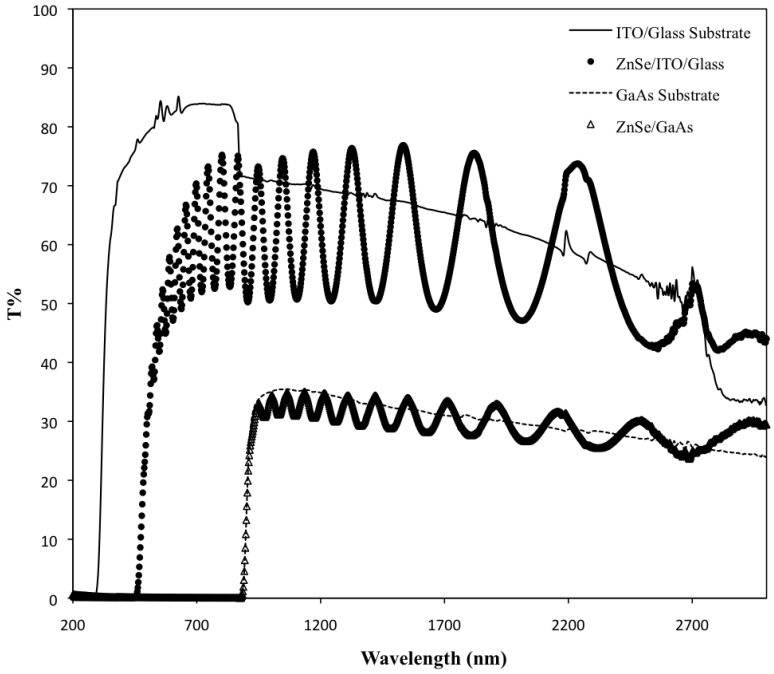


Figure 51. Plot showing optical transmission versus wavelength data for ZnSe thin films deposited on ITO/Glass and GaAs substrates and corresponding data for bare ITO/Glass and GaAs substrates

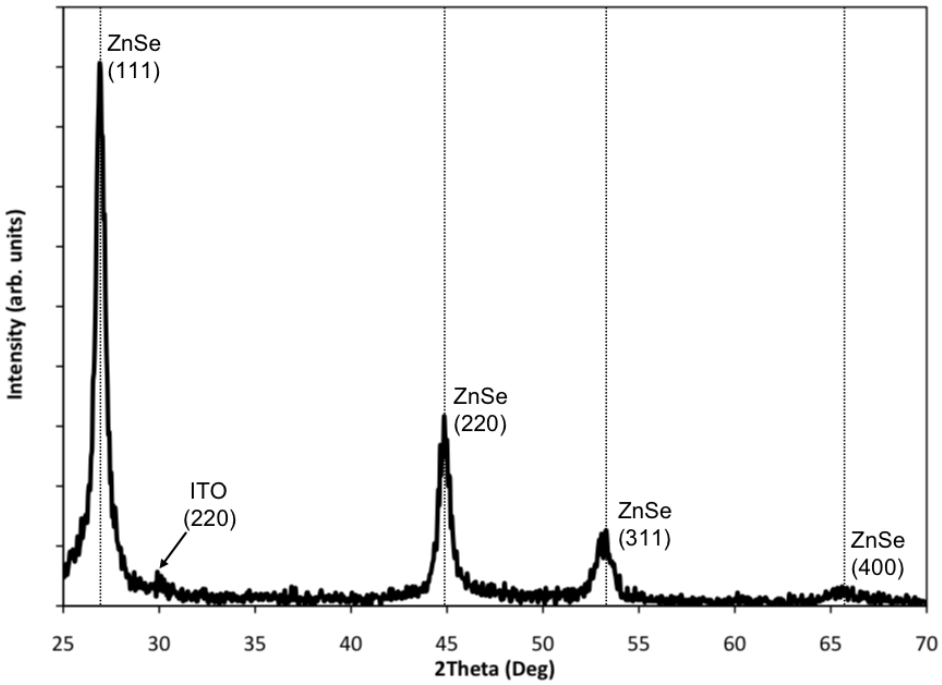


Figure 52. XRD glancing angle 2θ scan data of polycrystalline ZnSe thin film deposited on ITO/Glass substrate showing multiple ZnSe (cubic) diffraction peaks and weak ITO (cubic) diffraction peak

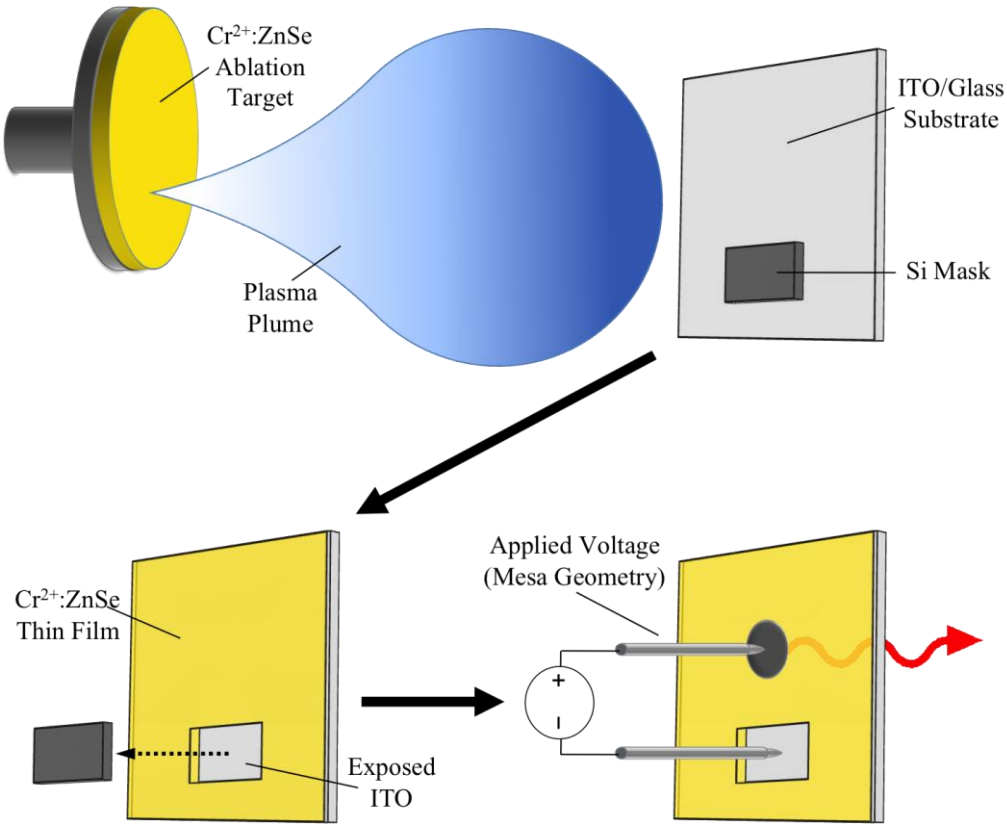


Figure 53. Schematic illustrating masking process implemented during thin film deposition leaving a portion of exposed ITO to act as the bottom electrode and deposited Ni contact atop the film to act as the top electrode for applying voltage across the Cr^{2+}:ZnSe thin film in mesa geometry for electroluminescence measurements

the deposited film as an electrode, rectangular Si masks (~1 cm^2) were installed on top of the ITO surface before thin film deposition (see Figure 53). Prior to the deposition process, both the mask and substrate were sonicated in acetone and methanol for ~10 minutes each, and then loaded onto the substrate holder for pumpdown. Thin film deposition was performed at a growth temperature of 450°C, which resulted in a polycrystalline Cr^{2+}:ZnSe film with a predominant (111) growth peak indicated by XRD glancing angle 2θ data (see Figure 52). Subsequent depositions were performed at different growth temperatures (500°C, 550°C), and the effect of temperature on the crystal orientation of the film was negligible within this range. Following thin film deposition, the chamber was allowed to

cool to room temperature before breaking vacuum to remove the sample for top contact deposition. The Si mask was removed, exposing the bare ITO to be used as the bottom electrode, and circular Ni contacts (0.4 cm^2) were deposited atop the Cr^{2+}:ZnSe film via magnetron sputtering for electroluminescence measurements.

7.2 Visible Electroluminescence in Cr^{2+}:ZnSe Thin Films

Before electroluminescence measurements were attempted, the structure was tested for electrical characteristics via EIS measurements. Applied DC voltages ranged from 10−20 V, resulting in corresponding current densities of 16.5−30 mA/cm^2 through the sample. A maximum current of 12 mA through the sample was achieved with an applied voltage and electric field of 16.7 V and 42 kV/cm, respectively. DC voltages were applied via a 2-point probe setup utilizing mesa geometry orientation with the sample mounted vertically on an optical collection platform (designed in-house) to be used in synchrony with a Fluoromax UV-VIS Optical Spectrometer to obtain electroluminescence spectra (see Figure 53).

To ensure proper functionality of the spectrometer, the emission spectrometer was calibrated using a water Raman calibration scan that utilized both the excitation and emission spectrometers of the device. However, since the excitation spectrometer component of the Fluoromax was not necessary for collection of emission via electrical excitation, an additional calibration procedure using an external 447 nm blue laser was implemented to assure proper alignment of the emission spectrometer. Before applying voltage across the structure, the sample-mounted platform was placed inside of the collection chamber of the spectrometer. To determine the optimal orientation of the sample to maximize collection of emitted light, a green light-emitting diode (LED) was powered

at the sample location and horizontal and vertical adjustments were made while monitoring counts with the emission spectrometer fixed at the peak wavelength of the alignment LED.

While applying voltage across the sample, the emission spectrometer was scanned through a wavelength range of 400−900 nm over a period of 6-12 hours for each value of applied voltage. To verify that the spectra obtained from the scans was indeed emission from the sample under electrical excitation, the emission spectrometer was fixed at the peak emission wavelength from the sample spectrum, and the applied voltage was toggled on and off by modulating the power supply until a square-wave-like behavior was observed from the detector (see Figure 54). Considering the low intensity of emission due to impact ionization expected in this geometry from such a thin film of Cr^{2+}:ZnSe, no signal was detectable until a voltage of 10 V was applied to the sample. As the applied voltage was increased within the range of 10−20 V, the intensity of emission increased (as shown in Figure 54) until device failure was realized at 19.2 V with an applied electric field of magnitude 48 kV/cm.

The electroluminescent emission spectrum obtained from the sample shows a broad peak centered at ~650 nm (~1.9 eV) that can be primarily attributed to deep centers due to crystal defects such as vacancies, interstitials, or other impurities in ZnSe [64]. Possible sources of emission in the detected range are attributed to defects such as Zn vacancies (2.06 eV), Cu impurities (1.95 eV), and Cl impurities (2.05 eV) in ZnSe [65,66].

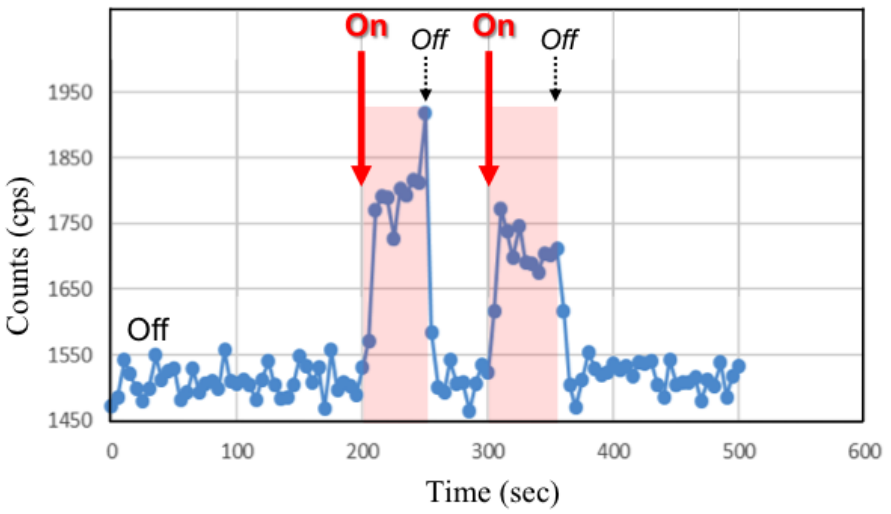


Figure 54. Detected signal from emission spectrometer of ZnSe/ITO/Glass sample under toggled electrical excitation (14.2 V, 10.6 mA, 26 mA/cm^2)

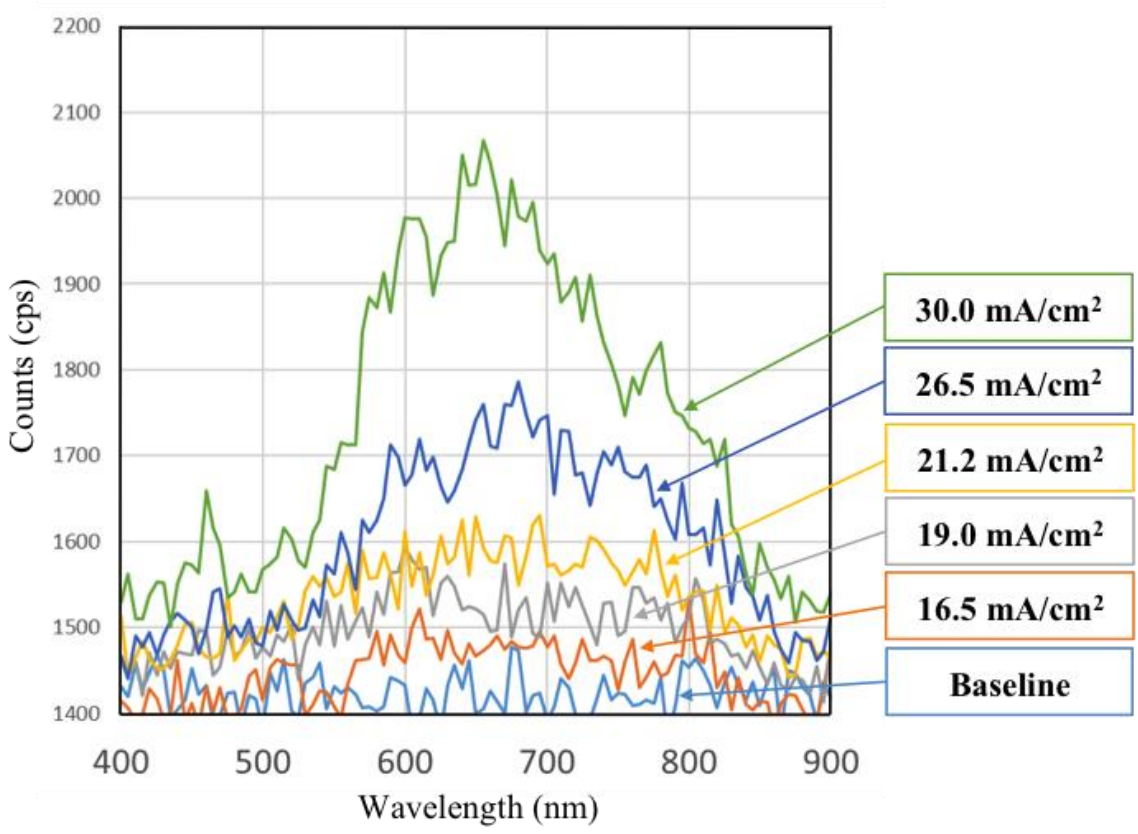


Figure 55. Electroluminescent signal versus emission wavelength of ZnSe/ITO/Glass sample under electrical excitation achieving the displayed current densities with increasing magnitude of applied voltage

A side peak of relatively low intensity, possibly attributed to the band-edge emission of ZnSe at 460 nm (~2.7 eV), is also observed to emerge with increasing applied voltage. However, considering luminescence measurements were performed at room temperature, the peak due to bandgap emission is expected to significantly broaden and shift towards longer wavelengths [67].

In addition, the acceptor nature of Cr^{2+} ions and the established contribution of holes to the valence band under optical excitation with photon energy greater than ~1.9 eV [74], as well as absorption by chromium ions due to sub-band excitation [73], could partially contribute to the low measured intensities of emission in this 400-900 nm spectral region. If there is quenching in this region due to free hole formation, these holes may subsequently be captured by a Cr ion, which will result in Cr excitation and possible emission of a photon in the mid-IR spectral region [72].

In addition to obtained visible luminescence, an electroluminescent signal was also detected within the 2-3 μm spectral range with a similar experimental setup utilizing low and high pass optical filters and a Germanium optical detector, but the intensity of emission was too weak to obtain a spectrum of the detected luminescence. This result is promising for future investigation of mid-IR emission from similar Cr^{2+}:ZnSe thin film structures. Possible future directions to explore include similar visible electroluminescence measurements as a function of decreasing temperature to observe the effect of temperature on the emission spectra, as well performing mid-IR electroluminescence measurements on similar Cr-doped samples with various thicknesses and multilayered geometries using an optimized infrared spectroscopic setup.

7.3 Summary of Results

Polycrystalline thin films of Cr^{2+}:ZnSe were deposited onto ITO substrates by PLD. Electrical measurements were made on the samples using a mesa geometry electrode system with an upper Ni contact deposited by magnetron sputtering and utilizing a region of exposed ITO as the lower contact. Current densities of 30 mA/cm^2 were attained at an applied DC bias voltage of 16.7 V and resulting electric field strength of 42 kV/cm across the sample. The sample was mounted onto a vertically-oriented optical collection platform to be placed inside of the collection chamber of a Fluoromax UV-VIS Optical Spectrometer in order to characterize emission within the wavelength range 400-900 nm due to electrical excitation of the sample.

While no detectable emission was observed for applied voltages below 10 V, a broad visible emission spectrum was detected and observed to increase in intensity with increasing voltage within the range of 10-20 V. While the structure showed stability with prolonged applied voltages within this range, failure/breakdown was eventually reached with an applied voltage of 19.2 V and corresponding electric field strength of 48 kV/cm. The broad electroluminescent peak centered around ~650 nm is primarily attributed to deep centers due to crystal defects including Zn vacancies, Cu impurities, and Cl impurities in ZnSe. However, a low intensity side peak observed at 460 nm is possibly attributed to the band-edge emission of ZnSe at room temperature. Low intensities of emission in this spectral range could indicate absorption by Cr ions, which based on the mechanism of absorption, could result in Cr excitation and resulting mid-IR emission. Using this same sample, a low intensity electroluminescent signal was detected within the 2-3 μm spectral range with a similar experimental setup utilizing low and high pass optical filters, but the

intensity was too weak to obtain a spectrum of the detected luminescence. This result is promising for future investigation of mid-IR emission from similar Cr^{2+}:ZnSe/ITO thin film structures.

CONCLUSIONS

8.1 Conclusions

Significant progress was made in this dissertation research towards the growth and characterization of essential components for the realization of a multilayered, mid-IR electroluminescent thin film device structure. Several studies were conducted on the effects of deposition parameters on the resulting crystal quality and defect density observed in resulting ZnSe-based thin films. Successful thin film growth of the ternary alloy, ZnS_xSe_{1-x}, was demonstrated on (100) GaAs substrates, and to our knowledge, is the first instance of the growth of this material via PLD. As epitaxial thin film structures are supposed to be ideal for realizing an electroluminescent device, conditions for epitaxy were explored in the ZnS_xSe_{1-x}/GaAs system by varying the sulfur concentration and substrate temperature during deposition.

Though most of the resulting ZnS_xSe_{1-x} thin films exhibited polycrystalline features via XRD data, several films displayed singular peaks aligned with an identical peak displayed by the bare GaAs substrate in XRD glancing angle 2θ scans. Further crystallographic characterization was performed on the films exhibiting epitaxial features via XRD $2\theta/\omega$ and rocking curve scans about the (400) GaAs diffraction peak. Pseudo-Voigt profiles were fit to the rocking curve data to aid in determining the FWHM and relative peak locations of the film and substrate, which are used to extract values for the

dislocation density and difference in lattice parameter of the films, respectively. The smallest average difference between lattice parameter of film and substrate was measured to be $\Delta a/a$=0.017% and was obtained for the $ZnS_{0.02}Se_{0.98}$ (x=0.02) sample deposited at a temperature of 450^{o}C, which was an unexpected result considering the well-established lattice matching properties of $ZnS_{0.06}Se_{0.94}$ (x=0.06) grown atop GaAs. Analysis of the rocking curve FWHM of the (400) GaAs growth peak reveals the sample with the lowest average dislocation density of D=2.87x10^{10} cm^{-2} to be the $ZnS_{0.06}Se_{0.94}$ (x=0.06) film deposited at a temperature of 450^{o}C. The measured dislocation densities and differences between lattice parameter of film and substrate were observed to increase with increasing film thickness of the illuminated region of the x-ray spot for a common sample. These characteristics are presumed to be consistent with epitaxially-oriented, polycrystalline structures, and are suggestive of regions of partial strain and varying degrees of relaxation as a function of film thickness and possible non-uniform distribution of sulfur atoms throughout the film structure during growth. While the films exhibiting epitaxy were initially thought to be single crystal in nature, the high dislocation densities measured, along with an observed variation in measured values for difference in lattice parameter and dislocation density dependent on the location of the x-ray spot on the film surface during XRD data collection, suggests the films to be epitaxially-oriented, polycrystalline structures.

A subsequent study was conducted on the effects of adding a Cr^{2+}:ZnSe layer of variable thickness at the GaAs interface in similar $ZnS_{0.1}Se_{0.9}$ structures. XRD analysis was performed to determine crystal quality and phase composition of all samples. While the $ZnS_{0.1}Se_{0.9}$ sample with no Cr^{2+}:ZnSe layer displayed prominent polycrystalline diffraction

features, an identical structure with a 150 nm Cr^{2+}:ZnSe layer added at the GaAs interface exhibited epitaxial features in the XRD data. As the thickness of the Cr^{2+}:ZnSe layer was increased, extraneous diffraction peaks emerged and became more pronounced with increasing thickness, but still retaining preferred growth in the (400) GaAs growth direction. Dislocation densities about the (400) GaAs diffraction peak in structure #1 and structure #2 were measured via Pseudo-Voigt fits to be 7.13×10^{11} cm^{-2} and 1.18×10^{10} cm^{-2}, respectively. The defect density measured from structure #2 was the lowest observed among all deposited samples in both studies, showing a vast improvement in crystal quality of the ZnS_xSe_{1-x} film with the implementation of the Cr^{2+}:ZnSe layer at the GaAs interface. Although polycrystalline films are expected at thicknesses necessary for utilization of ZnS_xSe_{1-x} films as waveguiding layers in a multilayered structure, electrical properties of these structures pose interesting non-linear I-V effects and high achievable current densities possibly capable of promoting luminescence under electrical excitation.

A study was conducted on the effects of the presence of a Cr^{2+}:ZnSe layer of varying thicknesses on multilayered thin film structures incorporating a 300 nm $ZnS_{0.1}Se_{0.9}$ waveguiding layer, (100) n-GaAs substrates, and Ni contacts. XRD analysis was performed to determine crystal quality and phase composition of all samples, showing a significant increase in crystal quality and epitaxial orientation in the sample with the added Cr^{2+}:ZnSe layer. As thickness of the Cr^{2+}:ZnSe layer was increased, deviation from epitaxy was observed with increasing thickness. Secondary “non-epitaxial” diffraction peak heights increased relative to the primary substrate growth peak with increasing thickness, along with an increasing value for calculated contact resistance, which indicates an increase in grain boundaries in structures as a function of increasing thickness of the Cr^{2+}:ZnSe layer.

EIS was performed to determine the electrical properties of the structures before and after an annealing process in forming gas background at 300°C for 5 minutes. The annealing process provided significant increases in conductivity by reducing dominating resistances originating from junction barriers. Effective barrier heights were determined from postanneal current-voltage data and showed an increase in effective barrier height and contact resistance due to collective grain boundary contributions with increasing thickness of the Cr^{2+}:ZnSe layer. Equivalent circuit models were used to calculate values of resistivity of the 300 nm $ZnS_{0.1}Se_{0.9}$ layer (1.95×10^5 Ω•cm) and the Cr^{2+}:ZnSe layer, which increased within the range $6.1\times10^6 - 2.5\times10^8$ Ω•cm with increasing layer thickness. This increase in resistivity of the Cr^{2+}:ZnSe layer is deemed to be due to the increase in the number of grain boundaries throughout the structures with increasing thickness. This study has proven valuable in verifying the need for implementing a ZnSe-based buffer layer at the GaAs interface to the proposed structure in Figure 1. The annealing process used in this study has shown to be effective in reducing the junction resistance of complex electrical multilayered structures, and the current densities obtained after annealing are promising signs for optoelectronic applications from similar structures.

Electroluminescent structures of polycrystalline thin films of Cr^{2+}:ZnSe were deposited onto ITO substrates by PLD. A maximum current density of 30 mA/cm^2 was attained at an applied DC bias voltage of 16.7 V and resulting electric field strength of 42 kV/cm across the sample. The sample was mounted onto an vertically-oriented optical collection platform and DC voltages were applied inside the collection chamber of a UV-VIS spectrometer. Under electrical excitation from 0-20 V, emission scans were performed over the range of 400-900 nm, and a broad visible emission spectrum was detected at a an

applied voltage of 10 V. The intensity of emission was observed to increase in intensity with increasing voltage within the range of 10-20 V, until device failure was reached at an applied voltage of 19.2 V and corresponding electric field strength of 48 kV/cm.

A broad emission peak was observed in the electroluminescence data centered around ~650 nm and is primarily attributed to deep centers due to crystal defects including Zn vacancies, Cu impurities, and Cl impurities in ZnSe. A low intensity side peak was observed at 460 nm, which is possibly attributed to the band-edge emission of ZnSe at room temperature. In addition, a low intensity electroluminescent signal was also detected within the 2-3 μm spectral range with a similar experimental setup utilizing low and high pass optical filters, but the intensity was too weak to obtain a spectrum of the detected luminescence. The realization of a Cr^{2+}:ZnSe-based structure displaying electroluminscence in the visible and mid-IR spectral range is a significant milestone for this dissertation research. These results show promise for achieving PLD-grown electroluminescent materials and structures, and have provided valuable electrical and crystallographic information on multiple components of a potential multilayered ZnSe-based thin film structure for mid-IR optoelectronic applications.

LIST OF PRESENTATIONS/PUBLICATIONS

PRESENTATIONS:

1. P. J. Marino, T. Konak, Z. R. Lindsey, V.V. Fedorov, S.B. Mirov, R. P Camata, "Nanostructured Cr2+:ZnSe-based Thin Films for Mid-IR Laser Sources," 2012 Fall Meeting of the Materials Research Society, November 25-30, 2012, Boston, Massachusetts.

2. Z. R. Lindsey, P. J. Marino, T. Konak, V.V. Fedorov, S.B. Mirov, R. P Camata, "Cr2+:ZnSe-based Thin Films for Mid-IR Laser Sources," Alabama EPSCoR Science & Technology Open House, April 5-6, 2013, Montgomery, Alabama.

3. Z. R. Lindsey and R. P. Camata, "Pulsed laser deposition synthesis of II-VI based ternary chalcogenide thin films" Tuskegee University Science & Technology Open House 2014, February 7-8, 2014, Montgomery, Alabama.

4. Z. R. Lindsey, M.W.Rhoades, V.V. Fedorov, S.B.Mirov, R. P. Camata, "Pulsed laser deposition of ZnS_xSe_{1-x} and its integration into multilayered Cr^{2+}:ZnSe structures for mid-IR electroluminescence," 82nd Annual SESAPS Meeting, November 18-21, 2015, Mobile, Alabama.

5. M.W. Rhoades, Z.R. Lindsey, V.V. Fedorov, S.B. Mirov, & R.P. Camata, "Carrier Concentration Control for n-Type Conductivity in Mid-Infrared Active Cr^{2+}:ZnSe Thin Film Structures," 82nd Annual SESAPS Meeting, November 18-21, 2015, Mobile, Alabama.

6. Z. R. Lindsey, M.W.Rhoades, V.V. Fedorov, S.B.Mirov, P.A. Kung, R. P. Camata, "Optimization of pulsed-laser-deposited ZnS_xSe_{1-x} for integration into multi-layered Cr^{2+}:ZnSe structures for mid-IR electroluminescence," Tuskegee University Science & Technology Open House 2016, February 5-6, 2016, Montgomery, Alabama.

7. Z. R. Lindsey, M. Rhoades, V.V. Federov, S.B. Mirov, and R.P. Camata, "Pulsed Laser Deposition of Relaxed ZnS_xSe_{1-x} Thin Films for Waveguiding Applications in Mid-IR Active Cr^{2+}:ZnSe Multilayered Structures." 2016 OSA ASSL Lasers Congress, October 30 – November 3, 2016, Boston, Massachusetts.

8. Z. R. Lindsey, M.W. Rhoades, V.V. Fedorov, S.B. Mirov, & R. P. Camata (2017). "Pulsed Laser Deposition of Epitaxial ZnS_xSe_{1-x} Thin Films for Waveguiding Applications in Mid-IR Active Multilayered Structures." 2016 Fall Meeting of the Materials Research Society, November 27- December 2, 2016, Boston, Massachusetts.

9. B.C. Chandler, Z.R. Lindsey, O. Gafarov, M.W. Rhoades, V.V. Fedorov, S.B. Mirov, & R.P. Camata; "Praseodymium- and Erbium-Doped Zinc Selenide Thin Films by Pulsed Laser Deposition for Middle-Infrared Laser Sources," 2016 Fall Meeting of the Materials Research Society, November 27 - December 2, 2016, Boston, Massachusetts.

10. Z. R. Lindsey, M.W. Rhoades, & R. P. Camata. "Co-Doping and Interface Defect Management in Optically Active Cr^{2+}:ZnSe Thin Films for Mid-IR Electroluminescent and Lasing Sources." 2018 Spring Meeting of the Materials Research Society, April 2-6, 2018, Phoenix, Arizona.

PUBLICATIONS:

1. Z. R. Lindsey, M.W. Rhoades, V.V. Fedorov, S.B. Mirov, & R. P. Camata (2017). "Pulsed Laser Deposition of Epitaxial ZnS_xSe_{1-x} Thin Films for Waveguiding Applications in Mid-IR Active Multilayered Structures." *MRS Advances*, 1-7. DOI: https://doi.org/10.1557/adv.2017.166

2. Z. R. Lindsey, M. Rhoades, V. V. Federov, S. B. Mirov, and R. P. Camata, "Pulsed Laser Deposition of Relaxed ZnS_xSe_{1-x} Thin Films for Waveguiding Applications in Mid-IR Active Cr^{2+}:ZnSe Multilayered Structures." Lasers Congress 2016 (ASSL, LSC, LAC), OSA Technical Digest (online) (Optical Society of America, 2016), paper AM5A.19.
DOI: https://doi.org/10.1364/ASSL.2016.AM5A.19

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