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A Low-Power Analog-Signal-Processing-Unit For Wirelessly-Powered Implantable Recording System

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COMPUTER ENGINEERING

ABSTRACT

Bio-electric signals convey information and phenomenon of the physiological activities of organisms, such as gene, protein sequences, neural, and cardiac rhythms. Various types of bio-electrical signals are extensively used for diagnostics as well as therapeutic interventions. Bio-electrical signals are low-amplitude, low-frequency and numerous unique properties (spiking, small oscillation, local field potential interference). The original signals amplitude is so small that directly lower the output resolution of the analog to digital converter (ADC). Furthermore, the detected signals are corrupted with, local field potential, white noise, system noise, and other interference, so the relevant information could be easily missed during the digitization. For such reasons, before the digitization, an analog signal processing unit is usually required. The one of the most challenge part in the analog signal processing unit design, for implantable signal recording system, is power consumption. The low-power consumption implants are one of the most efficiency ways to reduce the risk of tissue damage from the heat distribution. In this dissertation, a low-power analog signal processing unit for real-time bio-electric signals recording is performed. The analog signal processing unit has two major blocks, an amplifier filter bank for signals amplification and band selection, and a continuous wavelet transform filter for biosignals feature extraction. The amplifier-filter bank is inspired by the silicon neurons current sinking and charging feature. The technology, such as current bias and weak inversion CMOS, presented in the design significantly reduce the power consumption into the microwatt level. The new design method produces an analog continuous wavelet function filter with high performance, low circuit complexity and low-power consumption.

Keywords: low-power, amplifier, filter, analog signal processing, wavelet

DEDICATION

TO MY BELOVED PARENTS

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1. INTRODUCTION

Bio-electric signals (or ”electrical biosignals”) are the voltage potential of electric currents produced by the sum of electrical potential differences across tissue, cell or organ. Bio-electric signals convey information and phenomenon of the physiological activities of organisms, such as gene, protein sequences, neural, and cardiac rhythms. These signals provide us the information of the state of the living body. The monitoring and processing of real-time bio-electric signals can be essential for clinicians and researcher to diagnose a patient's health situation.

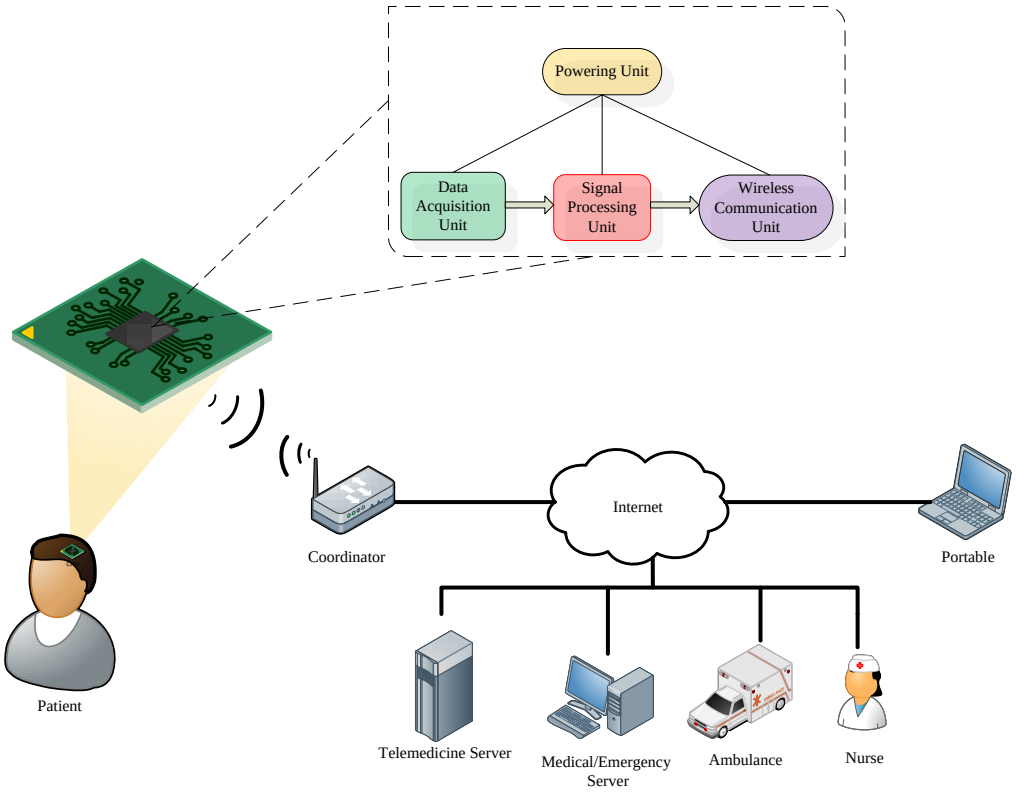

Figure 1: Wireless health care system

In order to obtain the bio-electric signals, the need of a bio-electric signals recording system is indispensable. A high-resolution implantable signal recording system captures the

detailed information of the vital physiological phenomena in the signal. The ultra-low-power implantable device with *in situ* sensor can capture a high-quality bio-electric signal. In emerging clinical applications including brain rehabilitation and epilepsy treatment, an implantable device shows great promise [**2**].

Many implantable bio-electric signals recording with wireless communication feature are studied in the recent years. The integrated circuit increases the number of recording channels, at the same time lower the power consumption. For the purposes of lowering the power consumption and achieving the large integration of the system, an application-specific integrated circuit is commonly pursued. A chip-based wireless implantable bio-electric signals recording system implanted in the patient's body offers real-time bio-electric signals measurement. The output results are sent to the coordinator through a wireless communication block in the system. The doctor and the nurse can monitor the patient through a computer (Fig. 1).

Literature review

Fig. 2 shows that the implantable devices start from the year of 1957. The medical implant device designed to replace a damaged biological organ or enhance a biological structure has a long history. In the 18^{th} century, Volta tried to stimulate the auditory system by using electricity through metal rods into the ears. In 1950, the stimulation of the auditory nerve by using a sinusoidal current was performed by Lundberg. At year 1957, Djourno and Eyries presented the theory of the cochlear implants with the function of stimulating the auditory nerve in the deafness.

The first implantable pacemaker was successfully implanted into an animal in 1958 [**10**] by Wilson Greatbatch and Dr. William Chardeack. After the Mr. Chardeack, Dr. Greatbatch and their coworkers' continuous works, the first human implant pacemaker was successfully developed [**11**] in 1960. At year of 1964, a "demand" pacemaker is reported by Barouh Berkovits. The "demand" pacemaker could stimulate the heart by sensing the heart whether is going to beating or not. The pacemaker can recognize and respond to intrinsic cardiac

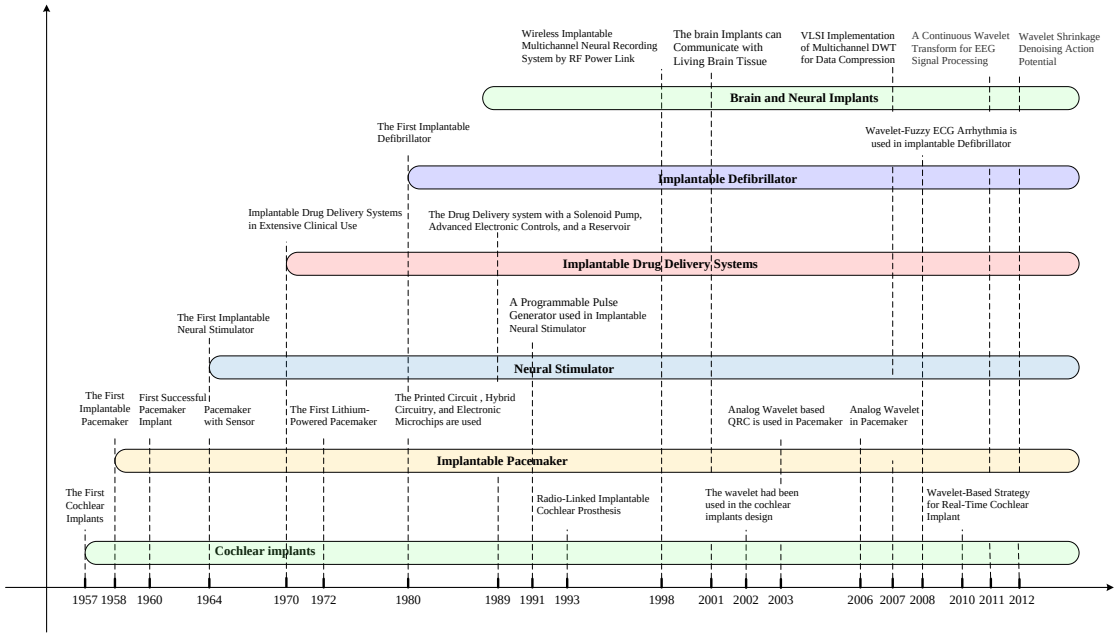

Figure 2: The diagram of the history of the implantable system.

depolarizations [**12**]. The first lithium-powered pacemaker was implanted in 1972 [**13**]. Blackshear's group used the pacemaker technology on the drug delivery system design in the early 1970s [**14**]. In 1972, an implantable blood pressure telemetry system for long term blood pressure monitoring with a passive transducer, band pass amplifier, phase detector, comparator, and RF-oscillator blocks have been proposed[**15**].

After successfully designed the implantable pacemaker to solve the heart rhythm problems, researchers started to make another device, defibrillator, to prevent death from a cardiac arrest. The first implantable defibrillator was reported [**16**] in 1980. The system was about 250 grams. The defibrillator could sense ventricular fibrillation from the sensor electrode implanted in the superior venae cavae and inject the electrical shock directly onto the heart to stop the ventricular fibrillation. Because of the improvements on the printed circuit board technology, large scale integration and the advancement of electronic microchips, the implantable devices become smaller and lower power consumption. The wireless powered pacemaker increased the safety by reducing the frequent operations for implantable battery replacement. The programmable pacemaker and defibrillator could handle the complex

scenarios of the patient's health status [**10**]. In 1970, the drug delivery implantable system was reported. On the year of 1989, a complicated drug delivery system with a solenoid pump, a reservoir, and electronic controls was developed by a joint group of the Johns Hopkins Applied Physics Laboratory and several other industries. This unit is powered by a lithium soluble cathode battery and fabricated by MiniMed [**17**]. An implantable neural stimulator was designed in 1991. The device delivers constant current electrical signals to the vagus nerve [**18**].

In the 1990, the wireless communication and signal processing were used in the implantable system to achieve data transfer in between the device and the monitoring system. An implantable cochlear prosthesis with wireless communication blocks using Radio-linked has been reported in 1993 [**19**]. This device with six processed speech data channels using frequency multiplexing is designed to embed in the cochlea. In the signal processing block, a filter bank is used to filter out six narrow band surface acoustic wave in the range of 72 MHz to 78 MHz with 1.2 MHz channel frequency band. In the wireless communication block, a portable transmitter and a receiver were designed. A new transmitter for implantable system was reported in 1996 [**20**]. A coil with a shape of the figure-of-eight was used in the signal transmission block. The coils were placed both inside and outside of the skin. The paper calmed that this method not only reduces the risk of the infections from the cord, but also enhances the coil noise reduction against the surrounding noise.

In order to further improve the neural recording system's performance, the multi-channel digital system was used. In 1998, a wireless implantable multichannel digital neural recording system was reported [**21**]. The recording system uses RF telemetry link to offer the wireless powering and controlling. The silicon electrode had an ability to capture $\pm$500 μV signal from axons. These signals were amplified by a 100 Hz to 3.1 KHz operating band amplifier before the digitization through a current mode 8-bit analog to digital converter (ADC). The report showed that the area of the chip without the RF interface circuit is 4*4 mm^2 with less than 2 mW power consumption at 5 V supply voltage and 2 MHz clock frequency. However, the chip area increases to 4*6 mm^2 after adding the RF interface. The

power consumption of the system is 90 mW. The brain implants, as well as neural implants, focus on establishing a prosthesis circumventing areas in the brain to detect a stroke or other brain diseases. In 2001, a brain implant was designed to communicate with living brain tissue [**22**]. The purpose of this device was designed for substitution of the lost cognitive function of the brain. The report shows the collective progress in the development of an analog/digital microchip to enable the function of the brain that damaged by a brain injury.

In 2002, the wavelet had been used in the cochlear implants design [**23**]. The author reports an application of an improved signal-processing for sound signal called bionic wavelet transform. The bionic wavelet transform reduced the advantage of channel number and the average stimulation duration. The new wavelet transform also improved the noise tolerance. The author only provided a simplified method of wavelet for the signal processing block in the cochlear implant. An on-chip implantable lock-in analyzer has been designed, fabricated and tested in 2002 [**24**]. This chip contained two frequency dynamical electrical bio-impedance analyzer, a low-frequency band with the range of 1 Hz to 8 KHz, and a high-frequency band of 1 Hz to 128 KHz. The processed signal was converted to an analog signal through a digital to analog converter(DAC).A digital wavelet transform circuit was integrated with the pacemaker application [**25**] in 2003. An analog wavelet transform filter was used in the signal processing block because of the low-power requirement in pacemaker. The pacemaker also contained an absolute value function circuit, a peak detector, and a comparator circuit. At the recent year, the wavelet transform has was used in the brain implants for ECG signal analysis [**26**].

A VLSI implementation on the multichannel discrete wavelet transform for brain implants was reported in 2007 [**27**]. The article focused on the implementation of the multilevel, multichannel discrete wavelet transform by using quantized filter and integer computation. The system has the power consumption of 76 μW and 0.22 mm^2 chip area with 32 channels 4-levels in 0.18 μm CMOS process. At the same year, the [**28**] Michigan State University group designed a scalable discrete wavelet transform for real-time signal processing. The VLSI based discrete wavelet transform works as a data compressor. In an example of the

paper, the system had 32 channels and four levels of decomposition. The fabricated chip had the size of 0.692 mm^2. It had 50.1 μW power consumption. In 2010, a group in the University of Texas at Dallas introduced the wavelet transform for the cochlear implants [**29**]. In 2011, a low-power, low-voltage and low-frequency bandpass filter implementation of a continuous wavelet transform was published. The group showed that the 7th order Gm-C filter based continuous wavelet transform filter with center frequencies ranging from 1 to 64 Hz with nanowatt power consumption[**30**].

The brain implants as one of the latest implants in the implantable device family are booming in the recent years. Many implantable bio-electric signals recording systems with wireless communication feature are studied in recent years. For the purposes of lowering the devices' power consumption, application-specific integrated circuits are typically pursued. The system in [**31**] has 32 neural recording channels grouped into four neural probes. Each probe has eight neural amplifiers and a 5-bit ADC. Without a wireless communication and signal processing blocks, the total power consumption of this recording system was reported to be 5.4 mW. The system reported in [**32**] had an amplification block, a data reduction block, an ADC block, and a wireless communication block. The wireless communication blocks supported 100 channels. The system uses 10-bit resolution on-chip ADC to digitize the signal. The chip was powered by inductive power link. The total power consumption was 13.5 mW. A 64 channels recording system was reported in [**33**]. The system had 16 parallel channels with 8 bits resolution. The power consumption of the core system was 14.4 mW.

2. THE STRUCTUE OF WIRELESS IMPLANTS

The basic structure of the implanted system usually includes four major units, powering unit, signal processing unit, data conversion unit, and wireless communication unit.

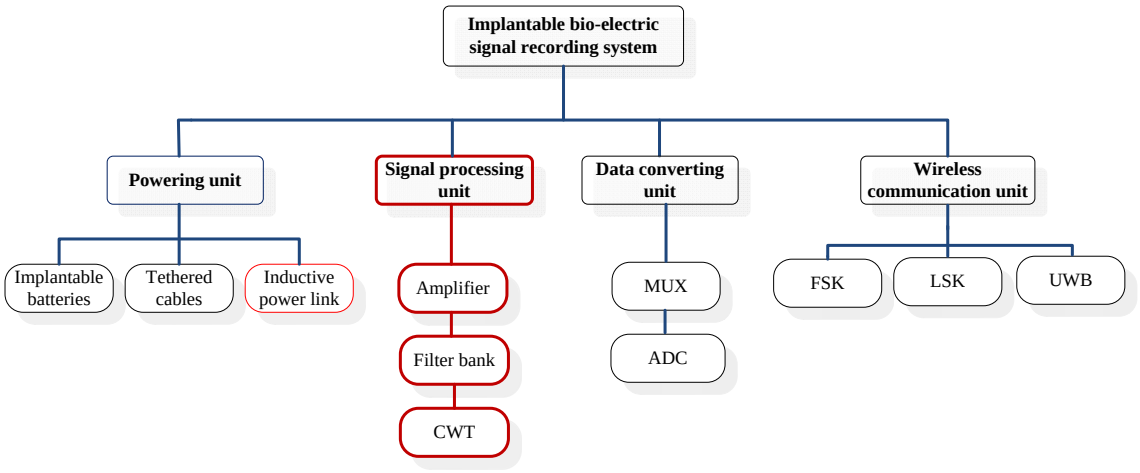

Figure 3: The basic functions block of the implant system.

The powering unit offers the voltage and current for the whole system. There are three primary methods for implantable device powering, the tethered cable, the implantable battery, and the inductive power link (Fig.3). The tethered cable is powered by an external power supply. The solid connection could provide a stable supply voltage and bias current. The data communication through the cable is low noise, high bandwidth, and high reliable. However, this approach might increase the skin and the tissue infection. It might heart the patient who wears the cable when he/she has body movement. Because of the high risk of the skin infection, the tethered cable is not considered as a proper powering method for the implantable device.

The implantable battery is a special battery that features the high power efficient, small size, and high reliability. Variety batteries are designed to meet the unique requirements of the different applications. Rather than the cable, the implantable battery eliminates the skin

risk of the skin irritation. However, it requires battery replacement. Without the tethered cable connection, the implant needs a wireless communication unit to communicate with an external device. Because of the high power consumption of the wireless communication unit, the implantable battery life decreases very fast.

The wireless power through the inductive power link is the third option for the implant device powering. Inductive power link has two loosely coupled resonating coils separated between the patient's skin. The primary side resides outside of the human body driven by a power amplifier or a power oscillator. The internal coil is placed beneath the skin to capture the power. In the biomedical implants design, the internal coil has the space limitation. In order to maximize the total power transfer efficiency, two coils should work in the resonant mode. The wireless power could avoid the skin infection from the tethered cable and frequent operations from the implantable battery replacement. The external side transfer the energy to the internal coil. The implants device send the modulated data trough the same coil to the outer side. The major cons of a wireless power are coil size, coils geometry, and limited power transfer capacity. The power transferability of the inductive power link limites the total power budget of the implanted system. The standard power transmit of the inductive power link is around 15 mW[**46**]. The signal processing unit, the data conversion unit, and the wireless communication unit must be operated in the low-power mode.

In the early 1980s' the signal processing unit in the implantable chip only had the function of amplification. Now, because of the large integrated circuit technology, the signal processing unit has the functions of amplification, filtering, continuous/discrete wavelet transform, Fourier transform, Hilbert transform, and so on.

The first critical block in the signal processing unit is the biopotential amplifier. The biopotential amplifiers are specially designed for biosignal with the common features of low bandwidth, low frequency, and low amplitude level. The amplitude of a neural spike signal ranges from 50 μV- 500 μV with the noise level of 5 μV - 10μV. The input-referred rms noise of the biopotential amplifier should be below 10 μV_{rms}. The power dissipation should be below 100 μW per channel in a multichannel system. The desired frequency bandwidth

of biopotential amplifier could be below 10 KHz, in order to cover the extracellular neural action potential. [**34**].

The second block is a filter or a filter bank. The filter bank extracts signals' features and power spectrum for compression and feature vector analysis. An analog signal processor manifests a bank of bandpass filters to identify different frequency channels in a hearing aid device. The reported bandpass filter based on automatic gain control amplifiers in [**38**] consumes 1.32 μW power for the center frequency of 1.18 KHz. The transconductance amplifiers and switched operational amplifiers, Gm-C and the switched-capacitor [**39**] [**40**] based filter structures have been considered to meet the stringent requirement of the system power budget. Because of the high noise of the filter structure and low amplitude of the input signal level, the conventional filter bank needs a high-performance preamplifier to amplify the signal. However, to maintain the low input-referred rms noise and a wider bandwidth, the power consumption of a biopotential amplifier could reach 10 μW or even higher regardless of the power consumption from the filter section [**35**]. Furthermore, the filter bank with multiple filter channels consumes additional microwatt power [**40**] that increases the power requirement of the implantable system. In order to save the power, the amplification and the filtering are combined into a single unit. The distributed bandwidth allocations are utilized to form a frequency selective amplifier-filter bank.

The third block of the signal processing unit is a continuous wavelet transform filter. The CWT is considered as one of the most useful technique in biosignal processing that offers the localization in both time and frequency for transients, aperiodic and non-stationary signals. The wavelet function facilitates the analysis of the frequency of the signal at any particular instance of time. By using different mother wavelet functions and dilation parameters, the CWT could provide the time-frequency analysis on the different types of biosignals. Because of this feature, CWT is widely used in the noise reduction [**42**], the spike detection [**43**], and the seizure detection [**44**]. The conventional CWT is based on software. The software based CWT requires a high data rate ADC to minimize data loss from the biosignal. The high performance ADC has a high power consumption [**45**]. However, for applications

requiring real-time processing, such as implanted or mobile biomedical devices, low-power consumption is a priority. Hence, the signal processing block should be implemented in hardware instead of software. Even in hardware-based implementation, analog circuits can offer reduced power consumption compared to the digital circuits [**47**]. CWT based on an analog filter implementation offers a power-efficient real-time signal processing [**48**].

Data conversion unit includes multiplexers (MUX) and ADC. MUX, also called a data selector, selects one of the several analog input signals and forwards the selected signal into an ADC. ADC converts a continuous signal into the digital numbers.

The digitalized signals are sent to the wireless communication blocks to communicate with an external device. The standard method of the wireless communication for an implantable device can be found as Load-shit keying (LSK), Frequency-shift keying(FSK), Amplitude-shift keying (ASK), and Phase-shit keying (PSK). Those methods are modulation schemes in which digital information are transmitted through the change of the carrier wave's amplitude, frequency or phase.

3. POWERING UNIT

In order to design the safety, high-efficiency and low-power implantable recording system, we have selected the wireless power through the inductive power link as the powering unit for our system. Figure 4 shows the block diagram of our wirelessly-powered implantable recording system. The block diagram of wirelessly-powered implant system is shown in Fig. 4. The powering unit, highlighted as red in the figure, is contrasted by and power oscillator (POSC), a pair of coupling coils in between the patent's skin and an internal rectifier circuit.

We have designed and published a prototype of the power oscillator based on the cross-couple oscillator and class-E amplifier in [**49**]. In order to increase the stability of the power oscillator design, an injection locking based power oscillator had been published in [**50**]. In the receiver part, we have used the zero voltage switching method on the rectified circuit design. A high-efficiency rectifier circuit is published in [**51**].

Robust Power-Oscillator

Fig. 5 shows the circuit schematic of the differential cross-coupled POSC used for the inductive-power-link system. It consists of cross-coupled MOSFETs to provide positive feedback, resonant LC tanks to generate resonant frequency, load network to ensure zero voltage switching of the cross-coupled MOSFETs and finally a bottom LC tank to filter out 2nd harmonic component of the oscillating frequency signal. Due to the cross-coupled MOSFET structure and the resonating LC tank, the circuit can generate high-frequency signal and obviate the need of a driver block. The free running frequency of the POSC can be depicted as,

$$f_{OSC} = \frac{1}{2\pi\sqrt{\frac{L_{RF}C_f}{2}}} \tag{3.1}$$

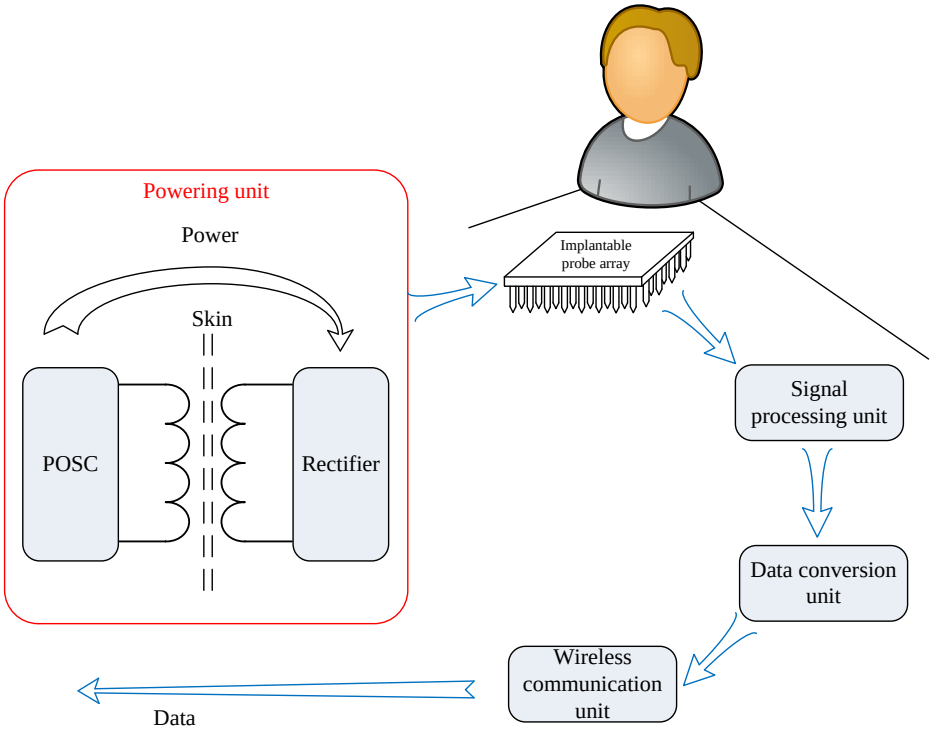

Figure 4: The block diagram of wirelessly-powered implant system with four major blocks. The powering unit is contrasted by and power oscillator (POSC), a pair of coupling coils, and an internal rectifier circuit.

where L_{RF} and C_f are the inductance and capacitance of the resonant tank circuit, respectively. The load network ensures zero voltage switching and helps achieving higher power efficiency.

Fig. 6 shows the setup of the POSC with an inductive-link coil system. The primary side of the link coils is energized by the POSC where the power is magnetically coupled to the secondary side in the resonant condition. Use of series resonance on the primary side and parallel resonance on the secondary side ensures better power transmission. An equivalent resistance value of 1 KΩ has been used to simulate the deliverable power to the sensor electronics inside the human body. Fig. 7 shows the simulation results of the POSC with a supply voltage of 3 V. It is clear that the differential cross-coupled POSC can maintain zero-voltage switching and achieve PAE of more than 90% for a load resistance of 400 . However, the coupling coefficient fluctuation disturbs the resonating resonant frequency

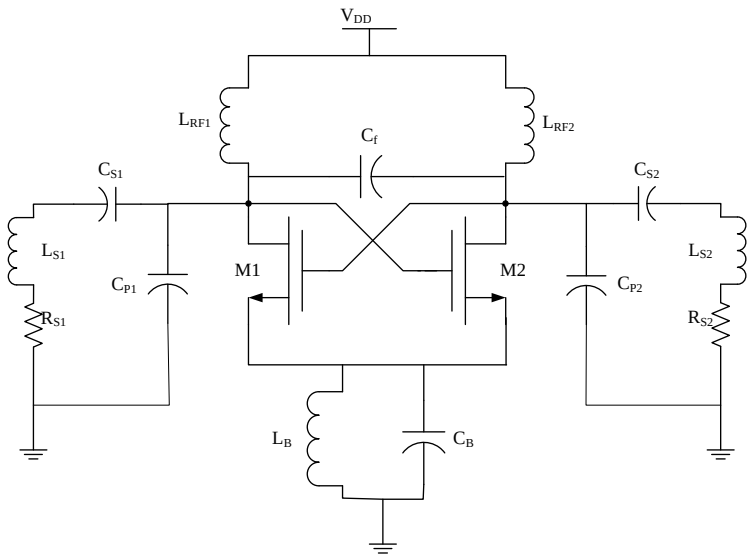

Figure 5: Differential cross-coupled power oscillator we have designed and published

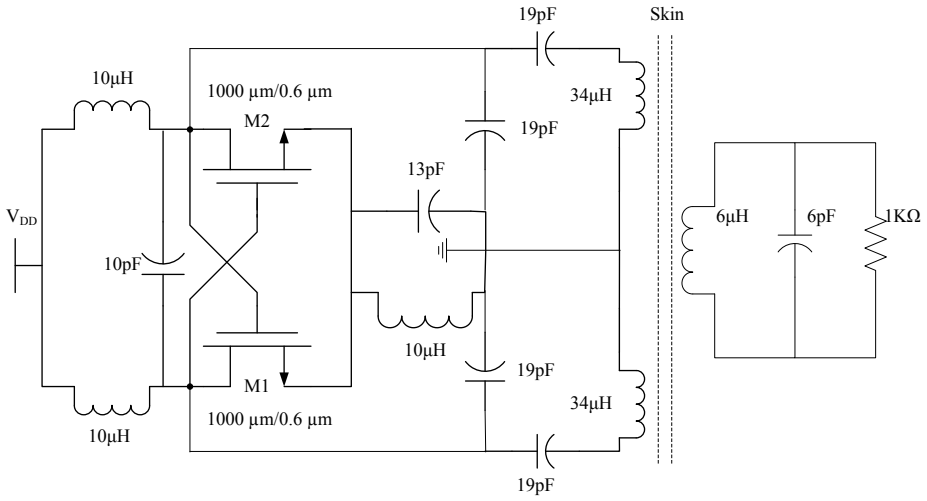

Figure 6: Inductive-power-link using differential cross-coupled power oscillator

of the resonant tanks and the load networks resulting in degraded efficiency. In order to overcome this problem, an injection-locking mechanism has been employed with the POSC structure.

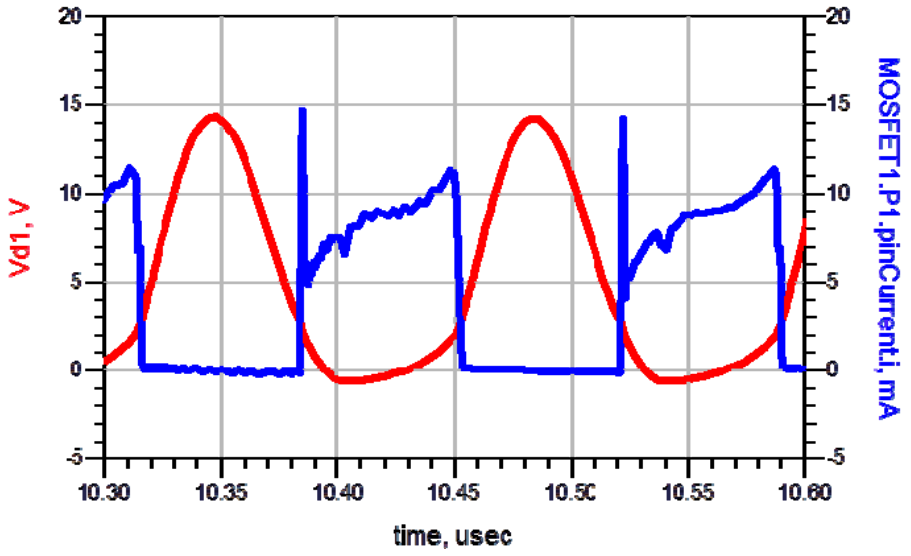

Figure 7: Simulated drain voltage and current wave shapes of the differential cross-coupled power oscillator

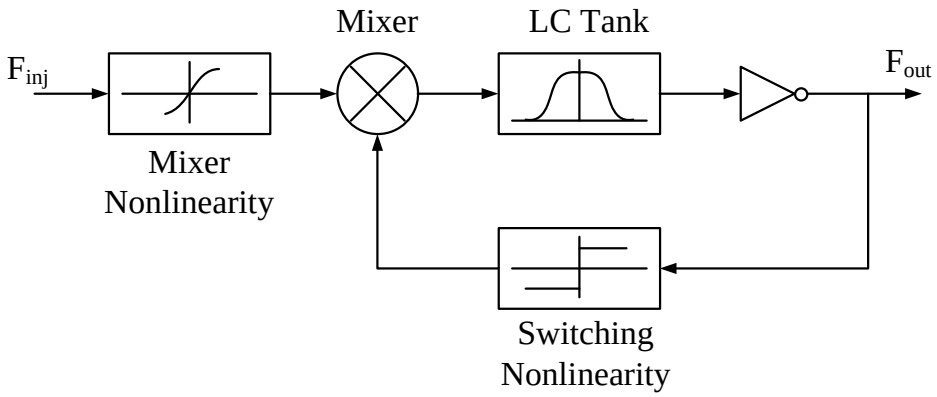

Figure 8: Behavioral block diagram of an injection-locked oscillator

The functional block diagram of an injection-locked oscillator has been shown in Fig. 8 . The core functionality of an injection-locked oscillator lies in a mixer block. Inside the mixer, the injection signal beats with the free running oscillator signal and the resultant harmonic signals are filtered out by the band pass filter of the LC tank. Only that harmonic

signal falls within the bandwidth of the bandpass filter comes out of the band pass filter, and the oscillator continues to oscillate at that frequency.

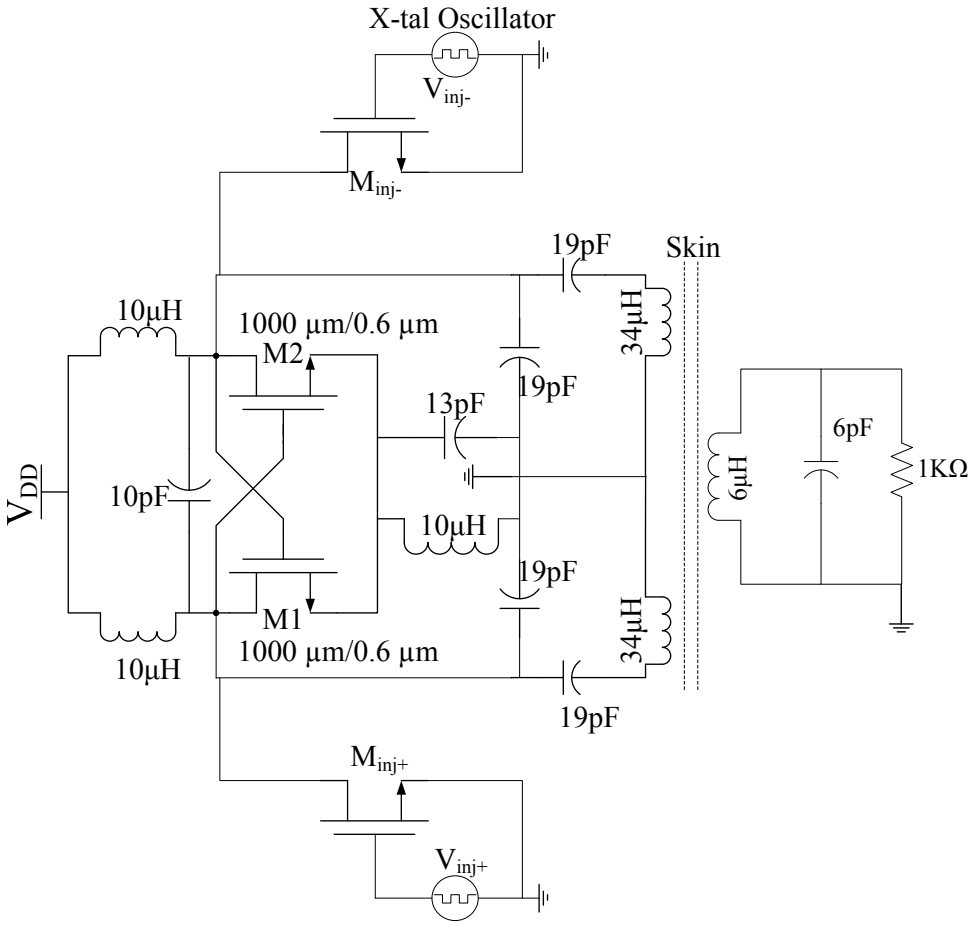

Figure 9: Inductive-power-link using differential cross-coupled power oscillator with injection locking

Fig. 9 shows the proposed injection-locked differential POSC where two parallel MOSFETs have been used to inject two differential current signals at the drain terminals of the cross-coupled MOSFETs of the main POSC. Under weak injection ($I_{inj} \ll I$), the phase variation of the output signal can be expressed as [**52**],

$$\frac{d\theta}{dt} = \omega_0 + \frac{\omega_0}{2Q}\frac{\pi}{4}\frac{I_{inj}}{I}sin(\theta_{ing} - \theta) \tag{3.2}$$

where Q is the quality factor on the resonant tank, $\omega_0 = 1/\sqrt{LC}$ is the resonance frequency, I_{inj} is injected current signal with a frequency ω_{inj} away from free running frequency ω_0, and I is the bias current of the oscillator. The gates of the injection MOSFETs are driven by two low-power crystal oscillators that do not increase the power consumption of the proposed circuit significantly. Under locking condition, the entire circuit works as a first order Phase Locked Loop (PLL) and the output frequency follows the frequency of the crystal oscillator. Due to the very stable frequency reference from the crystal oscillator, the injection-locked POSC can maintain a stable output frequency irrespective of the coupling coefficient variation from two inductive linked coils.

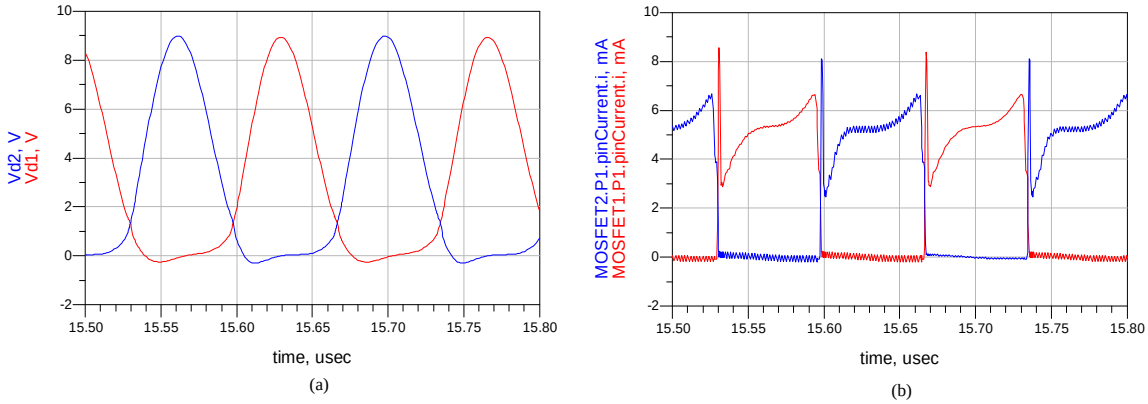

Figure 10: Drain voltage and current wave shapes of the injection-locked POSC for a nominal supply voltage of 3 V

In this work the proposed injection-locked different power oscillator has been simulated using 0.5-μm standard CMOS process to demonstrate the performance of the circuit with coupling coefficient variation. MOSIS provided 0.5-m CMOS models for MOSFETs and ADS simulator have been used to simulate the injection-locked POSC. The link coils and the passive components are envisioned to implement using commercial off-the-shelf (COTS) components. Fig. 10. Drain voltage and current wave shapes of the injection-locked POSC for a nominal supply voltage of 3 V When coupling coefficient equals to one the differential POSC without injection-locking shows more than 90% link efficiency. In this case all of the

LC tank circuits are working in the perfect resonance condition. However the variation of coupling coefficient is inevitable in real life. The changing coupling coefficient may create the main oscillation frequency to shift which causes the other three LC tank circuits to lose the resonant frequency.

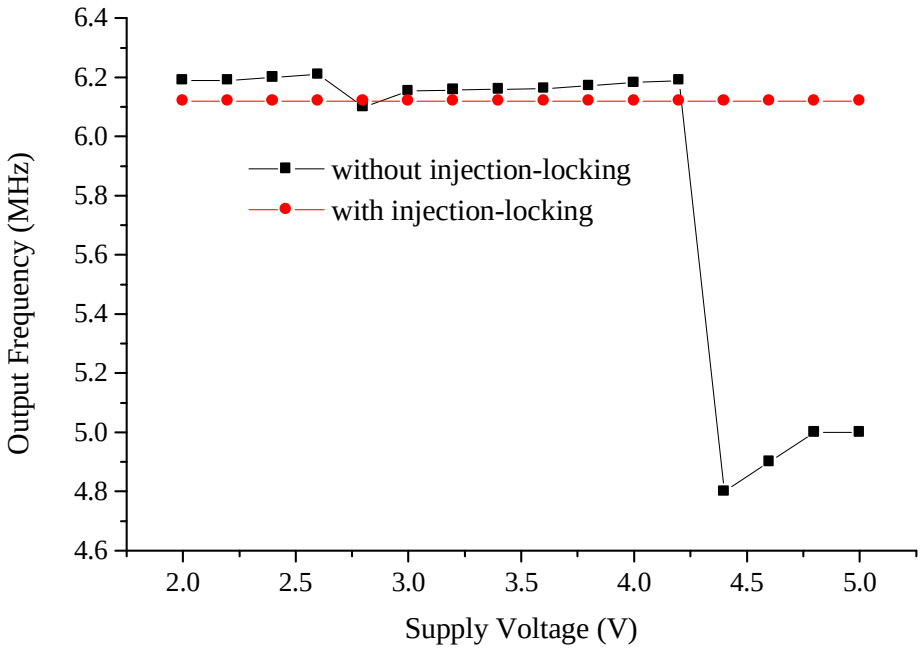

Figure 11: Supply voltage sensitivity of the POSC with and without injection-locking

Considering the case of a patients body movement, the coupling coefficient sensitivity of the POSC has been simulated using a sweep of 0.1 to 1 with 0.1 increment. To generate a stable output frequency and achieve a higher overall efficiency, injection-locking mechanism has been included with the POSC circuit. The drain voltage and current wave shapes for the injection-locked POSC has been shown in Fig. 10 where it is evident that the zero-voltage switching is still maintained. Two small aspect ratio parallel injection MOSFETs are used to inject two differential weak current signals at the drain terminals of the core oscillator. The gates of the injection MOSFETs are driven by two differential square wave pulses usually generated from a crystal oscillator. For simulation purpose two square wave voltage sources

are used to drive the injection MOSFETs. The frequency of the injection signal is chosen close to the fundamental frequency of the core oscillator. Under locking condition, the POSC follows the frequency of the injection signal and close-in phase noise becomes the phase noise of the injection signal. Due to the extremely low phase noise performance of the injection signal the frequency drift of the POSC is greatly reduced.

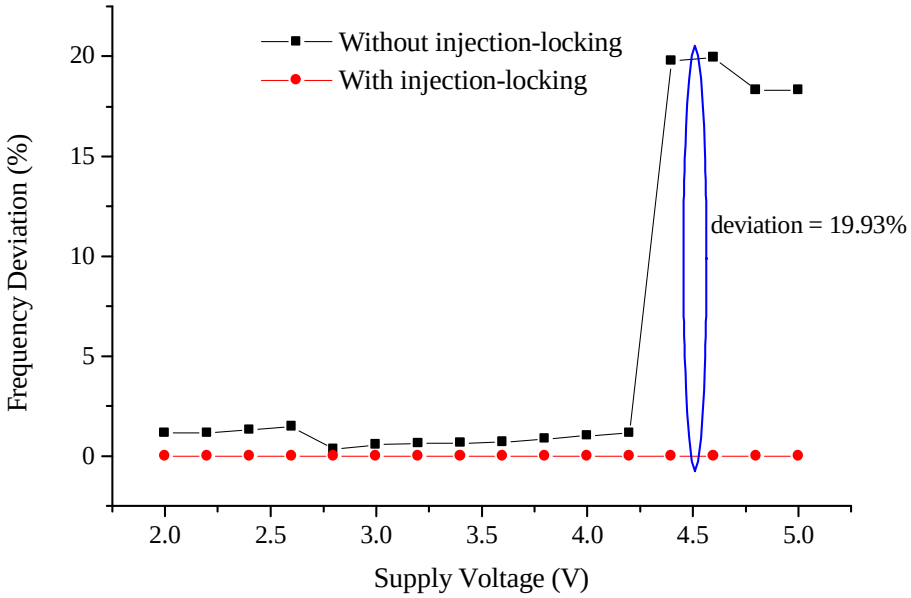

Figure 12: Percentage frequency deviation with the supply voltage variation

Fig. 11 shows the graphical plot of frequency variation with the variation of coupling coefficient. The black one with square mark indicates the frequency variation without injection-locking whereas the red one with circle mark indicates the variation due to injection-locking. With the variation of coupling coefficient, the frequency of the regular POSC varies in the neighborhood of the free running frequency until the coupling coefficient exceeds 1. The output frequency error is drastically increase by the decrease of the coupling coefficient. On the other hand with injection-locking, the output frequency maintains a stable 8.6 MHz frequency irrespective of the aforementioned coupling coefficient variation. Fig. 12 indicates the variation of the PAE with the coupling coefficient variation. It is evident from the figure

that for the different coupling coefficient the PAE of the POSC with injection locking is higher. However for a coupling coefficient is 1. The use of a voltage regulator can mitigate this problem at the expense of power loss and poor PAE from the POSC. Unlike voltage regulator, the injection-locking mechanism can work with extreme low-power consumption and keep the system in locked condition for a range of supply voltage variation. The red curve in Fig. 8 represents the percentage frequency change of the injection-locked POSC for the specified supply voltage variation. This indicates a performance improvement of the frequency stability by nearly 20% for a supply voltage variation by more than 1.2 V.

High Efficiency Cross-Coupled ZVS Rectifier

In the recent years, several rectifier structures have been reported in the literature to improve the power-conversionefficiency (PCE). The conventional full-wave bridge rectifier is not a superior option for implantable medical device, because of the low PCE. A bias-flip rectifier unit for energy harvesting from a piezoelectric harvester has been reported in [**53**]. A differential LC oscillator structure has been utilized as a rectifier with 75% efficiency targeted for biomedical implants [**54**]. The voltage drop and the power loss from the diode are inevitable for conventional full-wave bridge rectifier. To eliminate these problems, a new CMOS class-E differential circuit has been presented with Zero-Voltage-Switching (ZVS) characteristics to achieve 76% PCE [**55**]. A new active ('ideal') power diode with low voltage drop has been used in the rectifier circuit design. The power rectifier has 80% efficiency with 3.2 V input voltage [**56**]. Lam et al. presented a zero-threshold-active-diode controlled by four input comparators to design a rectifier unit. The rectifier has a turn-on delay of less than 2 ns and efficiency of 65% to 89% [**57**]. An integrated full-wave CMOS rectifier based on unbalanced-biased comparators presents more than 82% efficiency [**58**].

In this work, a differential class-E type ZVS CMOS rectifier is presented. The previously reported diode elements in [**55**] are replaced with inductors to enhance the PCE. The entire rectifier unit has been designed and simulated by using 0.5-μm standard CMOS technology.

Computer simulation reveals the superior performance compared to the previously reported works.

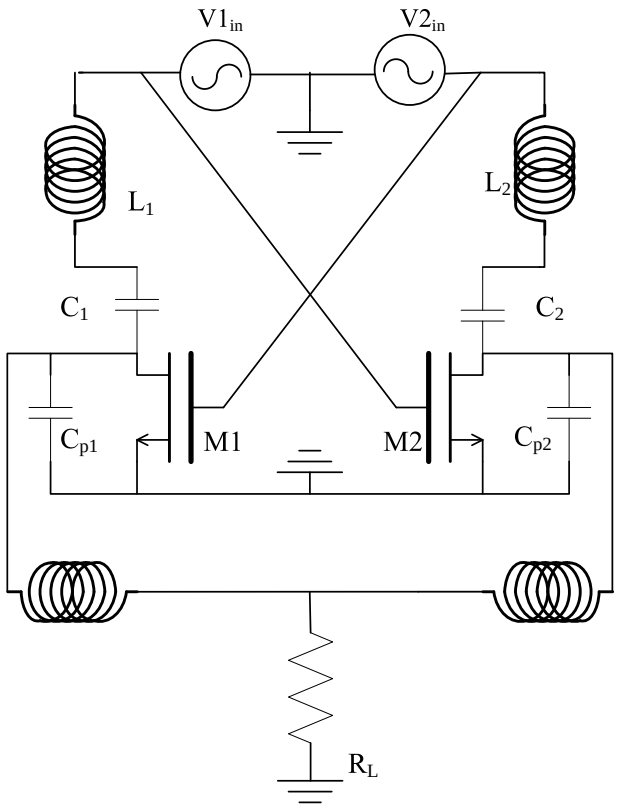

Figure 13: The scheme of differential Class-E zero-voltage-switching rectifier

The proposed class-E differential rectifier with ZVS MOSFETs is shown in Fig. 13 The differential circuit consists of two MOSFETs, two series resonant inductors and capacitors based LC tanks, two load capacitors C_{p1} and C_{p2}, two large inductors working as current sources at high frequencies, and a load resistor. The half circuit analysis has been used to describe the circuit behavior. The top series LC tank, L1 and C1, exhibits zero impendence at the resonance condition. However, it generates the $3/4\pi$ phase delay. When M1 is off, the current signal starts flowing into the load capacitor C_{p1}. When M1 is turned on by the gate signal, the current signal passes through the M1, and the capacitor starts to discharge. At this point the current signal and the voltage signals are sent to the load resistor. The

ZVS condition offers zero-power loss across the switch and improves the overall conversion efficiency. However, the passive components are considered not to consume any power.

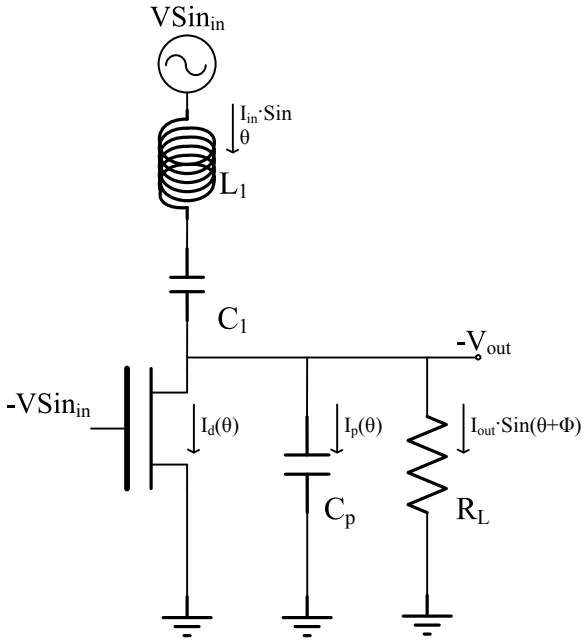

Figure 14: One side of the differential class-e rectifier

The key issue of the differential class-E ZVS rectifier circuit is to improve the PCE on the internal side of the implanted unit. The class-E based structure with ZVS has been chosen to provide maximum efficiency. The half circuit has been showed in Fig. 14. A high-speed switch MOSFET connects the sinusoid source through a series LC tank (L1 and C1), a tuning capacitor (C_p), and a load resistor (R_L). R_L represents the total impendence of the implantable microelectronics. Fig. 15 shows the idealized voltage and current wave shapes of the circuit. Referring to Fig. 14, the current through the circuit is given by,

$$I_{in} \cdot sin\theta = I_d(\theta) + I_p(\theta) + I_{out} \cdot sin(\theta + \phi) \tag{3.3}$$

When th switch is ON, i.e., for $-\pi < \theta < 0$, $V_{ds}(\theta) = 0$ and $I_p(\theta) = 0$. We got,

$$I_{in} \cdot sin\theta = I_d(\theta) + I_{out} \cdot sin(\theta + \phi) \tag{3.4}$$

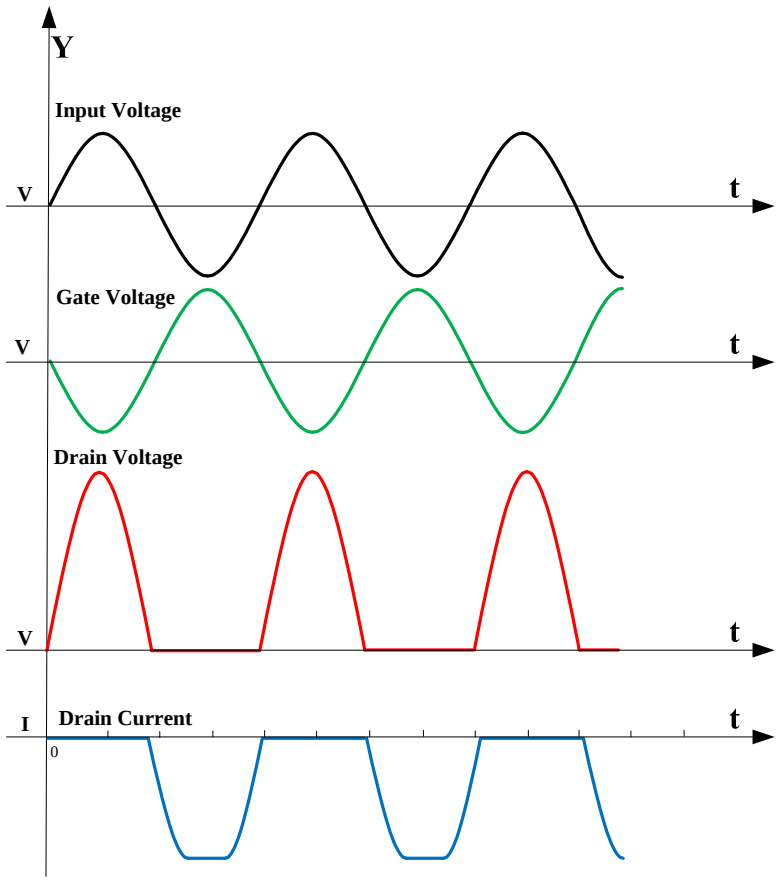

Figure 15: Idealized zero-voltage-switching waves

When the switch is OFF, i.e., for $0 < \theta < \pi$,

$$I_d(\theta) = 0 \tag{3.5}$$

The current through the shunt capacitance is given by,

$$I_{in} \cdot sin\theta = I_p(\theta) + I_{out} \cdot sin(\theta + \phi) \tag{3.6}$$

$$I_p(\theta) = I_{in} \cdot sin\theta - I_{out} \cdot sin(\theta + \phi) \tag{3.7}$$

The output impedance is given by,

$$Z_{out} = R_L \| \frac{1}{\omega \cdot C_p} = \frac{R_L}{1 + R_L \cdot \omega \cdot C_p} \tag{3.8}$$

Hence,

$$V_{ds} = Z_{in} \int I_p(\theta) d\theta \tag{3.9}$$

$V_{ds}(0) = 0$, so $V_{ds}(\theta)$ is given by,

$$V_{ds}(\theta) = \frac{R_L}{1 + R_L \cdot \omega \cdot C_p} \cdot [I_{out} \cdot cos(\theta + \phi) \cdot I_{in} - I_{out} \cdot cos\phi] \tag{3.10}$$

Imposing the ZVS condition given by $V_{ds}(\pi) = 0$,

$$cos\theta = \frac{I_{in}}{I_{out}}. \tag{3.11}$$

Imposing the ZVS, condition at which t $\theta = 0$,

$$sin\theta = -\frac{I_{in}}{I_{out}}. \tag{3.12}$$

From (3.11) and (3.12), we obtain,

$$\theta = \frac{3}{4} \cdot \pi. \tag{3.13}$$

From (3.9) and (3.13), we obtain,

$$\frac{V_{in_{peak}}}{2} = \frac{-5.54 \cdot R_L}{\pi(1 + \omega \cdot C_p \cdot R_L)} \tag{3.14}$$

The output impedance can be decomposed into two constituents - the real part and the imaginary part. Those two parts can be found by calculating the first order coefficients of the Fourier series of this signal. After equating the real and imaginary parts and using the resonance condition, the output power and the expression for the component values become as follows,

$$P_{out} = \frac{1}{2} \cdot I_{out}^2 \cdot R_L \tag{3.15}$$

The expression for load resistor is,

$$R_L = \frac{\sqrt{2} \cdot P_{out}}{\sqrt{2} \cdot P_{out} \cdot \omega \cdot C_p - I_{in}^3} \tag{3.16}$$

The expression of inductor L_1 is,

$$L_1 = \frac{2 \cdot P_{out}}{I_{in}^2 \cdot \omega}. \tag{3.17}$$

The expression of the tuning capacitor C_p is,

$$C_p = \frac{\sqrt{2} \cdot P_{out} - I_{in}^3 \cdot R}{P_{out} \cdot \omega \cdot R_L}. \tag{3.18}$$

The expression of LC tank capacitor C_1 is,

$$C_1 = \left(\frac{1}{2 \cdot \pi \cdot f} \right)^2 \cdot \frac{1}{L_1} \tag{3.19}$$

The simulated drain voltage and the corresponding drain current from the switching MOSFET are shown in Fig. 16. While the drain voltage excursion is positive, the drain current value is constantly zero. When the drain voltage stays at the zero level, the drain current excursion is going on. Because of the resonant ZVS MOSFET, the drain voltage has been shifted to the higher level. The small unexpected negative voltage pulse is due to the secondary harmonic interference from the final inductors. The bottom inductors and the tuning capacitor CP as a parallel LC tank generate some of the unexpected power loss. The proposed differential rectifier circuit can achieve more than 92% PCE for an input AC source of 7 MHz with peak to peak voltage of 2 V. In Fig. 17, the output voltage is around half of the peak input voltage, but the PCE is over 92%.

Table 1 shows the performance comparison of the proposed rectifier with the previously reported works. The proposed new class-E rectifier has the highest PCE of all. Table II shows the effectiveness of the design equations to design the proposed rectifier with the simulation results. In Table 2, the inductor L1 and the capacitors C1 and CP are considered to be implemented off-chip. Finally Fig. 18 shows the variation of the output power and the PCE of the rectifier with the variation of output voltage. The output power varies almost

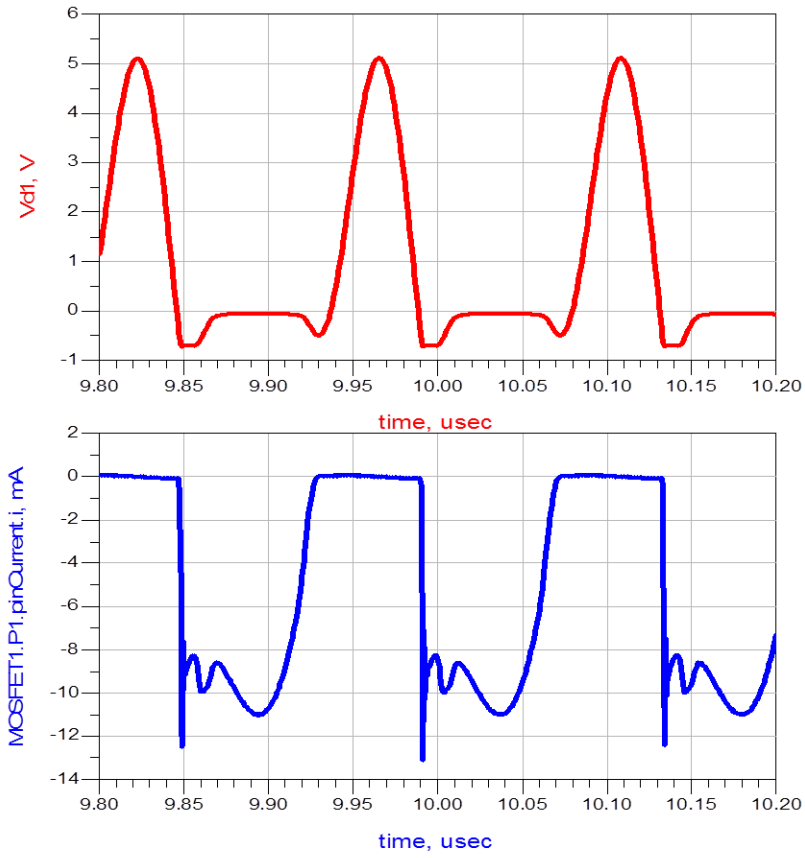

Figure 16: Drain voltage and drain current outputs of the rectifier circuit

Table 1: Performance comparison of the proposed rectifier with the previously reported works

	[54]	**[55]**	**[56]**	**[57]**	**[58]**	This Work
$V_{in_{p-p}}$	3 V	2 V	3.2 V	1.5 V -3.5 V	1.2 V -2.4 V	2 V
V_{out}	4.35V R=400 Ω	3V R=1$K\Omega$	3.02 V R = 10 $K\Omega$ 2.88V R=2$K\Omega$	1.27 V-3.45 V (unloaded) 1.2 V-3.22 V R=1.8$K\Omega$	1.13 V-2.28 V R=2$K\Omega$ 0.98V-2.08V R=100Ω	1 V R=100Ω
Freq.	7 MHz	8 MHz	5 MHz	13.5 MHz	200 KHz	7 MHz
PCE	75%	76%	80%	65%-89%	82%-87%	92%

linearly with the output voltage whereas the PCE varies linearly up to 1 V and after that it shows a level off pattern.

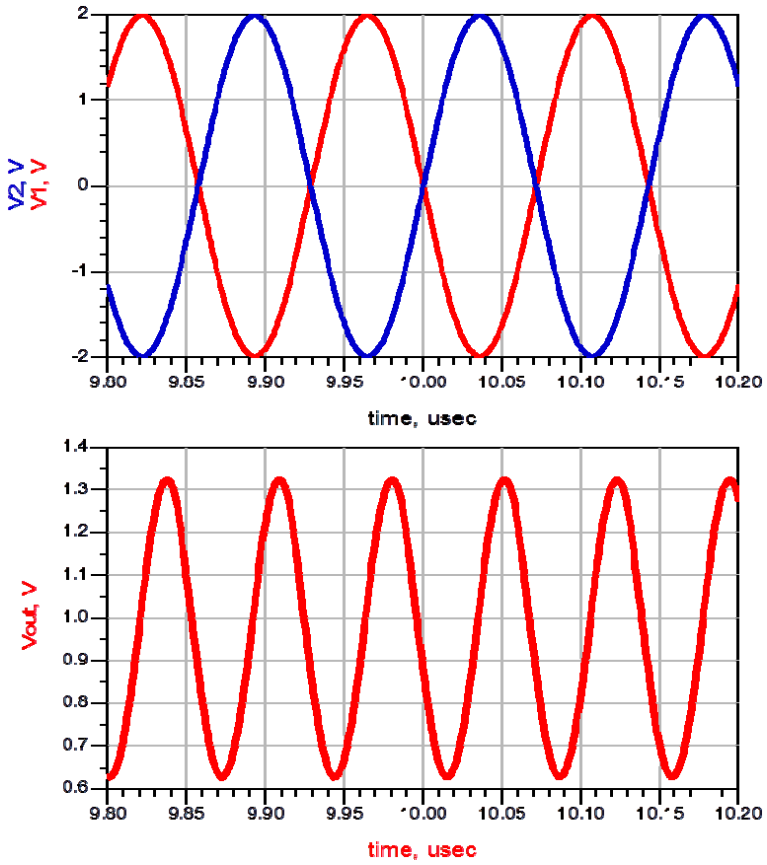

Figure 17: Rectifier input voltage and rectified output of the proposed rectifier unit

Table 2: Performance evaluation of the design equations with the computer simulation

	Value from equations	Value from computer simulation	Error
P_{out}	10 mW	11.4 mW	14%
I_{in} (peak to peak)	7 mA	7 mA	0
L1	9.28 μH	10 μH	8%
C1	56 pF	50 pF	12%
$Cp * RL$	2.20E-8	3.00E-8	36%
RL	1 kΩ	1 kΩ	0
Cp	22 pF	30 pF	36%

A modified class-E type CMOS differential cross-coupled rectifier circuit has been presented in this work. To estimate the components' values, design equations are presented

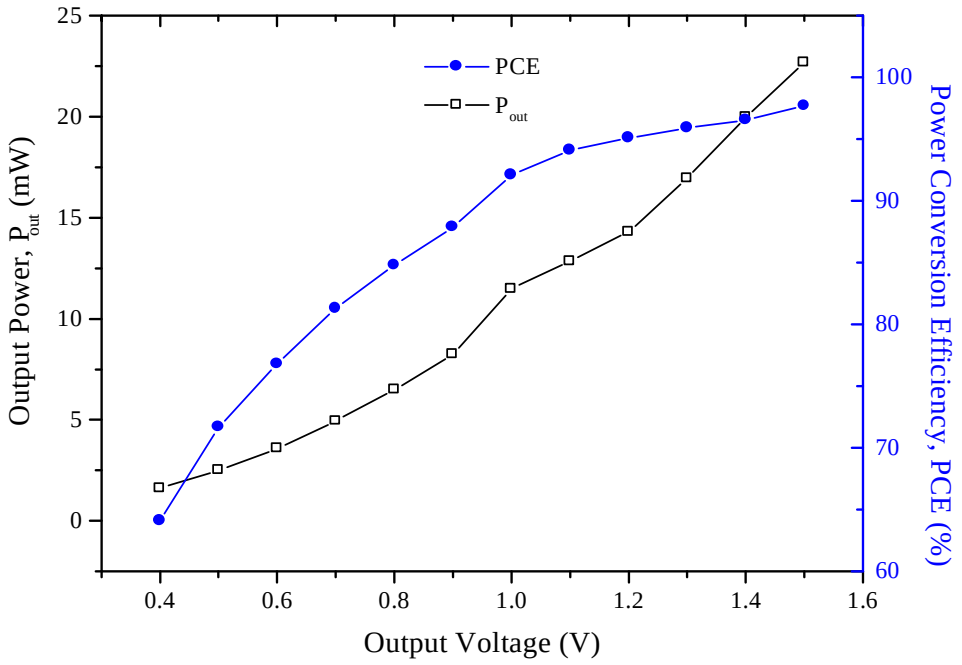

Figure 18: Variation of output power and PCE with the variation of output voltages

and verified with computer simulation. The theoretical values and the values from the computer simulation bear a close match. The ZVS structure eliminates the power loss from the transistor. In the proposed structure, the diodes are replaced by simple inductors to minimize the power loss from the last stage. Even though the final output voltage level is around half of the input peak level, the PCE remains higher than the previously reported diode ended rectifier circuits. Simulation results indicate a PCE of 92% for an input signal of 7 MHz, 2 V (peak) with a load resistance of 100 Ω.

4. SIGNAL PROCESSING UNIT

The second unit of the wirelessly-powered implant system is signal processing unit which is high lighted in the Fig. 19.

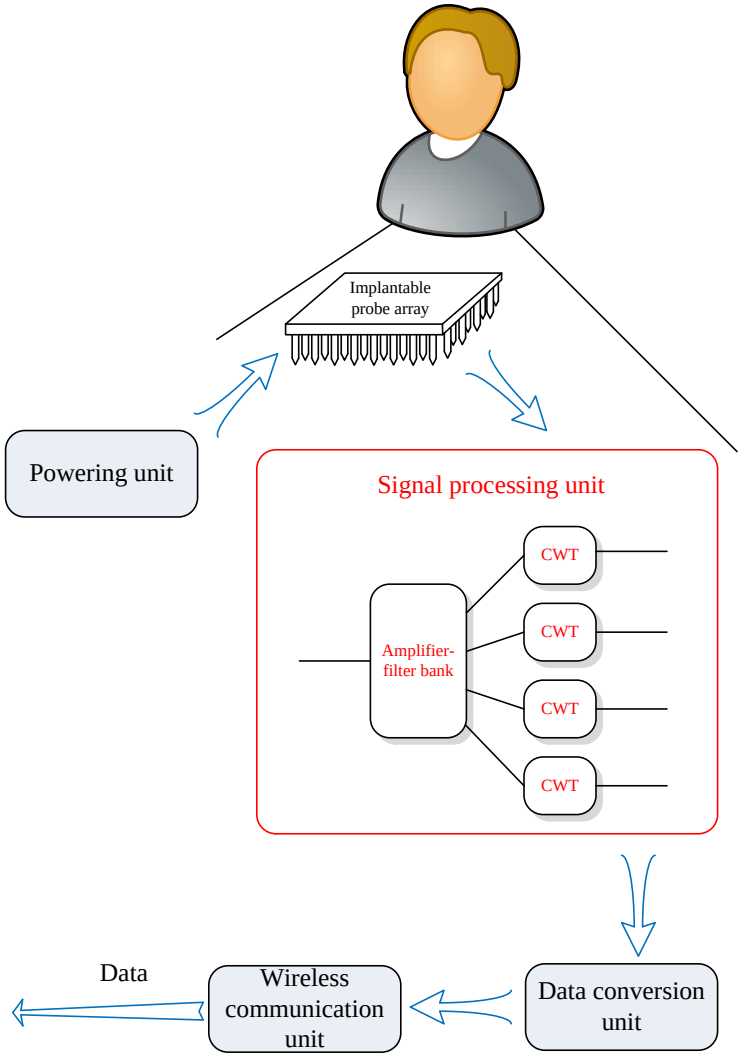

Figure 19: The signal processing as the second unit in the wirelessly-powered implant system offers multiply signal processing functions.

Signal processing unit is designed to process the information of vital physiologic phenomena in the bio-electric signals. The signal processing unit includes many blocks such as

low-noise amplifier, filter/ filter bank, and linear operations [**59**]. The low-noise amplifier is designed to amplifier the bio-electric signals captured by sensor array. The filter block function as the band selector filter out the desired signal band. The linear operations, usually based on software, provides signal analysis tools such as Fourier Transform, Hilbert Transform, and Continuous Wavelet Transform.

Problem statements and solutions

Statements of the problems

The small power budget for and high data volume are considered as two major challenges in the signal processing unit design. Due to the high power requirement and the circuit complexity, the conventional signal processing unit in the implantable signal recording system only has very basic function such as low-noise amplification and ADC blocks[**60**][**59**]. The signal analysis such as Fourier Transform, Hilbert Transform, Continuous Wavelet Transform, feature extraction, and data compression are based on the software. In this scheme a high resolution ADC is required to ensure the accuracy of the sampled data. However, due to the limited bandwidth of the wireless communication unit in the implantable recording system, the signal need to be compress and processed before the data converting unit.

The Fig. 20 shows the power budget of different unit in the implantable system [**34**]. The wireless communication unit is the most power consumption units in the system. The wireless communication unit could consume around 50% of total power. 30% of power is allocated to the data conversion unit. Only 20% of total power is used in the signal processing unit.

Fig. 21 shows the block diagram of conventional implantable recording system. The reported works showed that a signal amplifiers power consumption could reach ten μW [**34**]. Furthermore, the power consumption of the filter bank can reach 262 μW [**61**]. The state of the art of the implantable recording system has around 100 channels [**32**]. If we

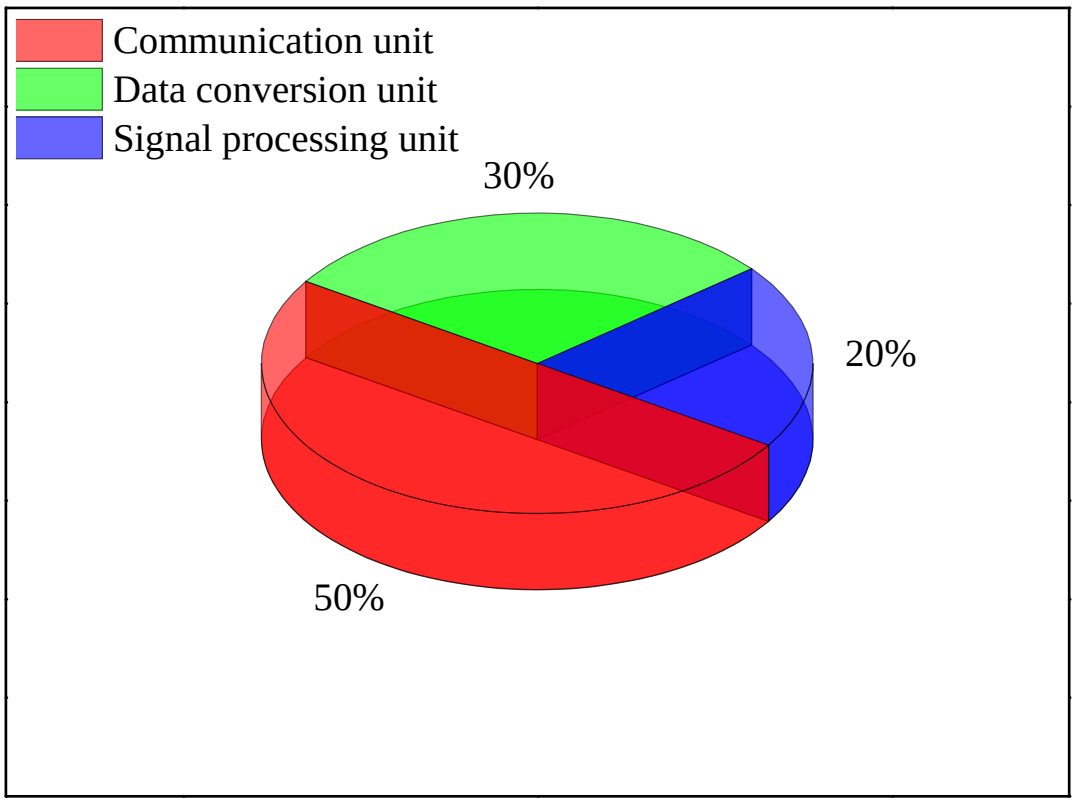

Figure 20: The power allocation for signal processing unit, data conversion unit, and communication unit

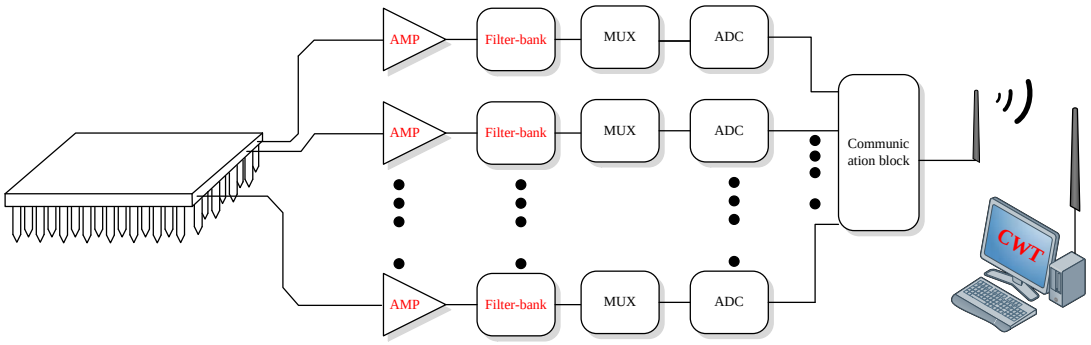

Figure 21: The block diagram of implantable recording system

have 100 channels in our system, the total power consumption can reach as high as 27 mW with only amplifier and filter bank in the signal processing system. However, the average power transmit from the inductive power link is around 15 mW[**62**]. The power allocated

to the signal processing is only 20% of the total transmitted power. To support around 100 channels signal processing unit by using 3 mW power is a major challenge.

Furthermore, A typical recording experiment with a 100 micro-electrode array sampled at 25 kHz per channel with 12-bit has 30 Mbps data rate [**63**]. But 30 Mbps is beyond the reach of state-of-the-art wireless telemetry [**63**]. The data compression is needed before the data conversion unit.

Proposed solutions

To achieve a low-power design, we have two primary solutions. The first is using the bio-inspired circuit structure. The second is the combination of the two function blocks to produce amplification and filter at the same time. The second method is to use the neural feature to make a low-power circuit design. The silicon neural based on the current sinking and sourcing with log-domain function could generate different spike signal with ultra low-power consumption. The block with gain and delay could be used in the amplifier and filter design.

In order to reduce the data value, spike detection is used. Instead of sending whole data, the system could send the spike pulse which contains the most information of the signals [**64**]. In order to achieve the spike detection and data compression, a wavelet transform is used in this design. However, The conventional wavelet is based on software that requires high data rate ADC to minimize the loss of information of the signal. The high performance ADC usually has high power consumption [**45**]. Furthermore, for applications requiring real-time processing, such as implanted or mobile biomedical devices, low-power consumption is a priority. Hence, the signal processing block should be implemented in hardware instead of software. Most of the hardware based wavelet transform is based on digital which also depends on the performance of ADC. In order to lower the power consumption of the hardware-based wavelet transform, many research groups start to build low-power analog wavelet transform. The analog circuits can offer reduced power consumption compared to the digital counter [**47**].

Silicon neural

The silicon neural structure greatly decrease the power consumption by using the current sourcing and sinking method. The amplifier and filter design is the based on our proposed work [**1**]. In order to deep understand the structure of the neural inspired circuit design, the structure of the bursting silicon neural design and simulation is showed below.

Introduction

Neuron is the fundamental unit of neuromorphic computation, an energy-efficient information processing technique in living organisms. A single neuron is connected to thousands other neurons. Communication among neurons takes place via electrical signals that are produced as a consequence of the variation of the neuron membrane conductance for the various ions present in a cell.

The formulation of the electrical model of the neuron by Hodgkin and Huxley in the early 1950s facilitated the development of the silicon neuron. This has spurred active research in the area of neuromorphic engineering, such as mimicking the physiological behavior of the human brain, etc. Several implementation of the silicon neuron have been reported in the literature, ranging in complexity from simple current-to-spike frequency generators to multicompartment, multichannel models, and ranging in density from a single neuromorphic neuron to arrays of tens of thousands neurons [**65, 66, 67**].

Bioinspired and neuromimetic designs are the two existing design approaches in neuromorphic engineering. The bioinspired design is based on a minimal neuron model, which facilitates ease of implementation, reduced power consumption and flexibility to create large complex networks. On the other hand, the neuromimetic design is a more detailed implementation of neurobiological phenomena. Neuromimetic design addresses issues in neuroscience such as comprehension of central pattern generator [**68**], rhythmic motor control [**69**], or vision processing [**70**]. Compared to the bioinspired design, the neuromimetic design is much more accurate in mimicking the behavior of a real neuron.

Complexities in the implementation of neuromimetic design led researchers to investigate bioinspired silicon (Si) neuron architectures. Several bioinspired Si neuron architectures have been reported, leaky-integrate-and-fire model, oscillatory neuron structures, Izhikevich neuron model, to name a few. The leaky-integrate-and-fire model, based on current stimulus, cannot imitate the cortex and the behavior of a real neuron. Oscillatory neuron structures cannot produce all the spiking and bursting patterns that are observed in a real neuron [**71**]. The Izhikevich neuron model, considered one of the most effective neuron model, is able to generate different neuronal signals, and has been implemented with only 14 MOSFETs [**72**]. However, the parameters in the Izhikevich neuron model lack biophysical meaning. Hence, bioinspired silicon neuron have not been effective in reproducing the dynamics of a real neuron.

The H-H model is a neuromimetic design that provides the most accurate representation of the ionic dynamics [**73**]. It models the Si neuron based on the ionic flow through the neuron membrane with a set of equations. A conductance based H-H type neuron model has also been reported, but the implementation requires a large number of transistors [**74, 75**].

In this paper, a novel four-channel Si neuron architecture based on the bursting H-H model is presented. The four-channel Si neuron reflects the relationship between the internal current flow and the variation of the output membrane signal [**76**]. The proposed structure highly improves the power efficiency by eliminating the duplicated current flow present in [**74, 75**]. The proposed Si neuron can produce four different neuronal signals - spiking, spiking latency, bursting, and chaotic signals. The entire structure is designed using 0.13 μm standard CMOS process. The proposed design achieves ultra-low-power consumption due to the use of fewer transistors and subthreshold region operations of the transistors. The simulation results indicate that the total power consumption of the proposed Si neuron cell is only 43 nW.

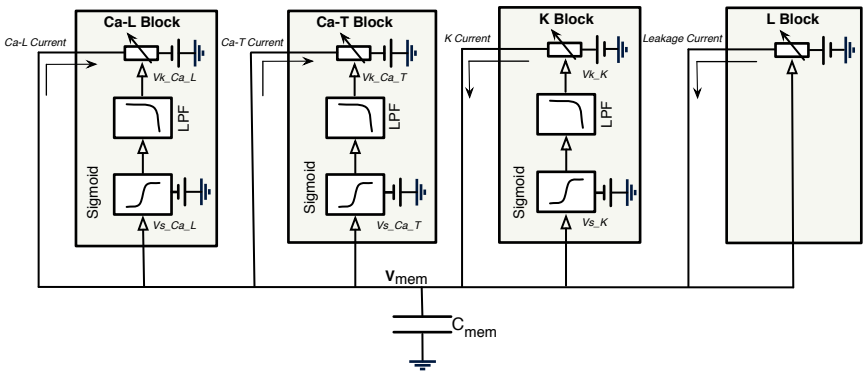

Figure 22: Hodgkin-Huxley Bursting Neuron model. LPF stands for low-pass filter.

Proposed Si Neuron Architecture

A H-H model Si neuron includes four ion channels. Fig. 22 shows the functional block diagram of a single Si neuron model. The first channel carries L-type Ca current. The second channel carries a rapidly inactivating T-type voltage sensitive Ca current. The third channel carries a voltage-sensitive K current and the fourth channel carries a leakage current, which represents the rest of the ionic flows in the cell. The leakage current and the K channel current charge the membrane capacitance, while the L-type and the T-type Ca channels discharge the membrane capacitance. The membrane voltage is a function of the sum of the ionic currents in the four channels that flow into the membrane capacitance C_{mem}.

The voltage across the membrane capacitance is

$$C_{mem}\frac{dV_{mem}}{dt} = I_{leak} + \sum_j I_j, \tag{4.1}$$

where C_{mem} is the membrane capacitance, V_{mem} is the membrane potential, and I_j is the current from the j^{th} ionic channel associated with the corresponding channel voltage-dependent-conductance.

The H-H model contains two different states - 'activation' and 'inactivation' [8]. In this design only activation state is used to define the ionic currents. The currents due to

voltage-dependent conductance is

$$I_j = \bar{g_j} \,.\, \tilde{m_j} \,.\, (E_j - V), \tag{4.2}$$

where $\bar{g_j}$ is the maximal conductance, $\tilde{m_j}$ is the normalized state variable, and E_j is the reversal potential.

The ionic currents are generated by the difference in membrane potential from the reversal potentials v_{Ca-L}, v_{Ca-T} and v_K [**65**], across the conductances g_{Ca-L}, g_{Ca-T} and g_K.

$$I_{Ca-L}(v) = g_{Ca-L} \,.\, m_{\infty-L} \,.\, (V - v_{Ca-L}) \tag{4.3}$$

$$I_{Ca-T}(v) = g_{Ca-T} \,.\, m_{\infty-T} \,.\, (V - v_{Ca-T}) \tag{4.4}$$

$$I_K(v) = g_K \,.\, n \,.\, (V - v_K) \tag{4.5}$$

$$I_{leak} = g_L \,.\, (V - v_L) \tag{4.6}$$

$$\frac{dm_L}{dt} = \frac{m_{\infty-L}(v) - m_{\infty-L}}{\tau_{m_{\infty-L}}} \tag{4.7}$$

$$\frac{dm_T}{dt} = \frac{m_{\infty-T}(v) - m_{\infty-T}}{\tau_{m_{\infty-T}}} \tag{4.8}$$

$$\frac{dn}{dt} = \frac{n_\infty(v) - n}{\tau_n} \tag{4.9}$$

$$x_\infty = \frac{1}{1 + \left(exp\frac{V_x - v}{X_x}\right)}, \quad x_\infty \in [m_{\infty-L}, m_{\infty-T}, n] \ . \tag{4.10}$$

The equations (3)-(10) represent the mathematical model of the H-H silicon neuron. The conductances used to generate the ionic currents are modulated by the set of gating

parameters, $m_{\infty-L}, m_{\infty-T}, n \in [0,1]$ which represent the opening and closing to the ionic channels in the neuron cell. g_{Ca-L}, g_{Ca-T}, g_L and g_K are the transconductances in Ca-L, Ca-T, K and leakage channels. The functions $m_{\infty-L}(v)$, $n_\infty(v)$ and $m_{\infty-T}(v)$ are the steady-state activation functions. v, V_x and X_x represnt the membrane potential, the zero crossing point of the sigmoid function and the slope of the sigmoid function, respectively. v_{Ca-L}, v_{Ca-T}, v_K and v_L are the threshold voltages in the Ca-L, Ca-T, K, and the leakage channels. τ is the time constant generated from the log domain filter.

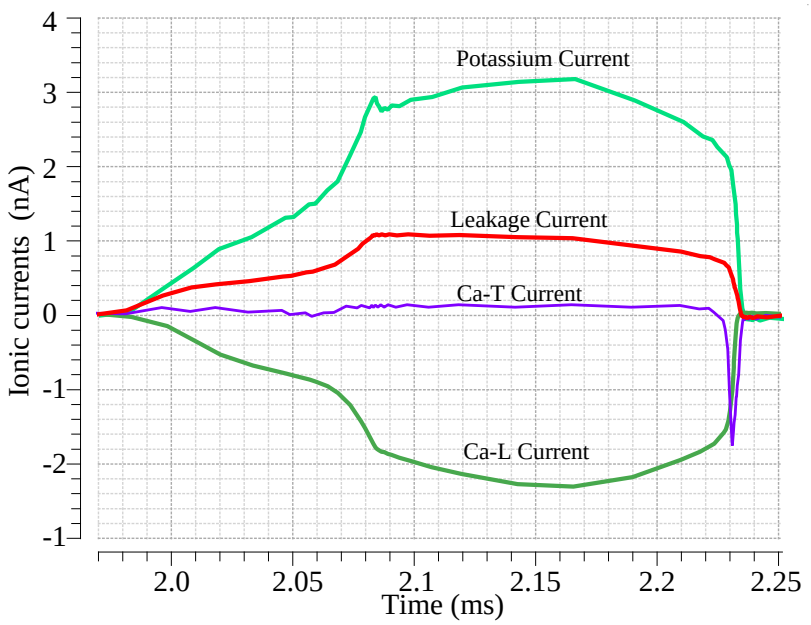

Figure 23: Transient outputs of different ionic current channels.

Fig. 2 depicts the variation of ionic currents with time for a single spike generation. Initially, the membrane capacitor has no charge. The leakage current slowly charges this capacitor to the certain potential, which opens up the potassium (K) channel. The potassium current increases with the increasing membrane potential. As a consequence of high membrane potential, the L-type calcium (Ca) channel is turned on, and the L-type current starts to discharge the membrane capacitor. However, as the charging process is faster than the discharging process, the membrane voltage continues to increase. When

the membrane potential finally reaches a certain value, the T-type Ca channel opens and completely discharges the membrane capacitor. This process is repeated.

In the proposed Si neuron implementation, each ionic channel is constructed using a sigmoid function block, a log-domain filter, and a linear transconductor. A brief description of all of these building blocks along with the different ionic channels are presented in the following sections.

The sigmoid function behavior can be implemented using a subthreshold MOSFET-based differential amplifier. In this work, two types of sigmoid functions with different conductance behaviors are used. The T-type Ca current is active at a low threshold voltage, and becomes inactive rapidly, thereafter. Hence, a fast-response sigmoid function is required to implement the T-type Ca current channel. A gate controlled MOSFET differential amplifier-based sigmoid function (Fig. 24 (top)) serves that purpose. The body controlled MOSFET-based sigmoid structure, with a wider range (Fig. 24 (bottom)), is used in the L-type Ca block and in the potassium block.

For a MOSFET operating in subthreshold region, the drain current can be approximately expressed as

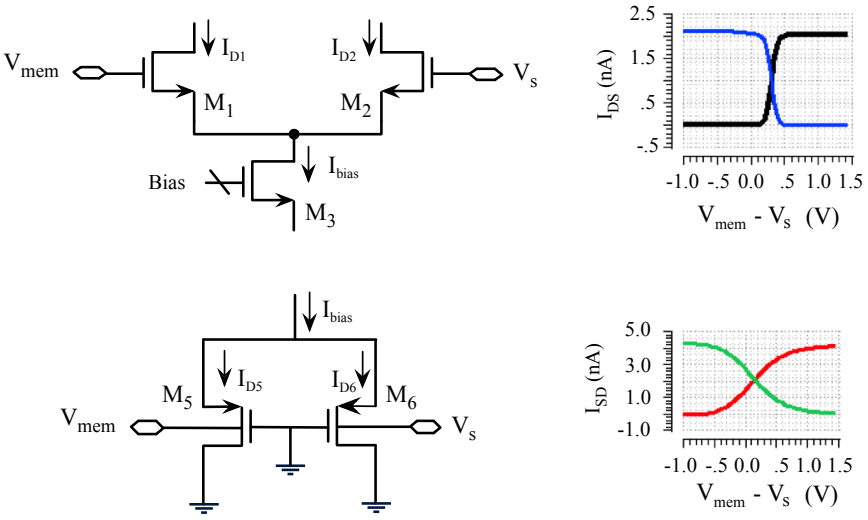

Figure 24: The gate controlled (top) and body controlled (bottom) sigmoid function.

$$I_D = I_o \left(\frac{W}{L}\right) e^{\frac{V_{GS}}{\kappa V_T}}, \tag{4.11}$$

where I_o, $\left(\frac{W}{L}\right)$, κ, V_{GS}, and V_T represent the technology current, MOSFET aspect ratio, non-ideality factor, gate-to-source voltage, and the thermal voltage ($=\frac{kT}{q} \approx 25mV@27C$) respectively. For the MOSFET pair in Fig. 3 (top), the device currents can be expressed as

$$I_{D_1} = \frac{I_{bias}}{1 + e^{\frac{V_{mem} - V_s}{\kappa V_T}}} \tag{4.12}$$

$$I_{D_2} = \frac{I_{bias}}{1 + e^{-\frac{V_{mem} - V_s}{\kappa V_T}}} \ . \tag{4.13}$$

From (4.12) and (4.13) , it is evident that the sigmoid characteristics is achieved from a MOS differential pair working in the subthreshold region.

In a similar manner, we can derive the expression for current in the body driven sigmoid-function circuit as,

$$I_{D_5} = \frac{I_{bias}}{1 + e^{\frac{V_{mem} - V_s}{V_T}}} \ . \tag{4.14}$$

Comparing (4.12) and (4.14), it can be seen that the subthreshold current in the gate driven sigmoid function is dependent upon κ, while the body-driven sigmoid function is not. For a typical value of κ of about 0.7, the gate driven sigmoid function shows a faster response than the body driven sigmoid function.

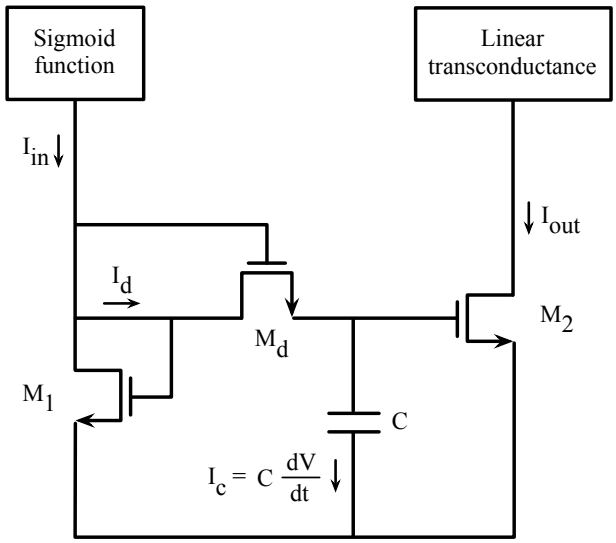

Figure 25: Schematic of the log domain filter.

The operation of the log-domain filter can be explained using the translinear circuit principle. The circuit schematic of the log-domain filter is shown in Fig. 25. The current flowing through M_1 is defined by

$$I_{in} - I_d = I_{out} \tag{4.15}$$

where I_d represents the current through the M_d with zero gate-to-source bias voltage.

The capacitor current can be expressed as

$$I_c = C\frac{dV_{GS2}}{dt} = I_d \ . \tag{4.16}$$

Using (4.11), (4.15) and (4.16), we get

$$\frac{dI_{out}}{dt} = \frac{I_{in} - I_{out}}{\frac{CV_T}{\kappa I_d}} \ . \tag{4.17}$$

From (7), (8), (9) and (4.17), the time constant τ can be expressed as

$$\tau = \frac{CV_T}{\kappa I_d} \ . \tag{4.18}$$

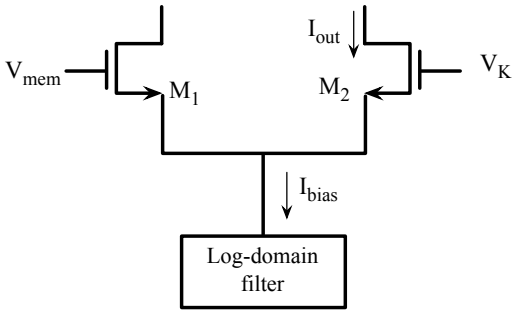

Figure 26: Linear transconductance based on linear region of sigmoid function.

The main purpose of using linear transconductance is to control the output current with the variation of membrane voltage. The current expressed in the equations (3) - (6) can be implemented using linear transconductance. The linear region of a regular sigmoid function is used as the linear transconductance. Fig. 26 shows the circuit schematic of the linear transconductor where the controlling parameter is the bias current of the tail MOSFET. Fig. 27 shows the linear transconductor I-V plot. The output current of the linear transconductor for subthreshold region operation can be approximated as

$$I_{out} = I_{bias} - I_{bias} \cdot \frac{\kappa}{V_T} \cdot (V_m - V_K) \ , \tag{4.19}$$

where V_T denotes thermal voltage.

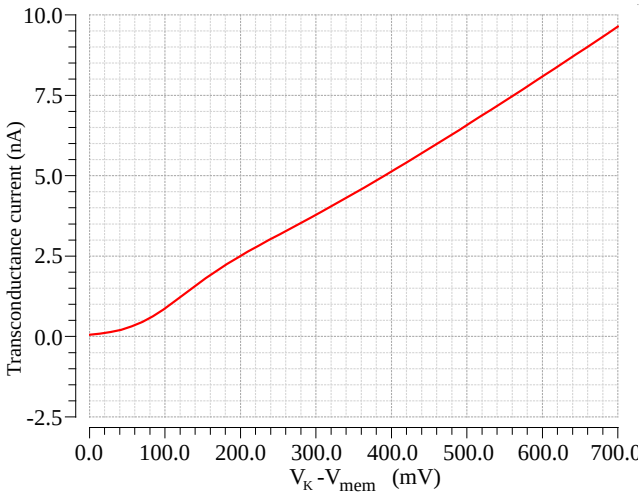

Figure 27: Variation of output current of the linear transconductor.

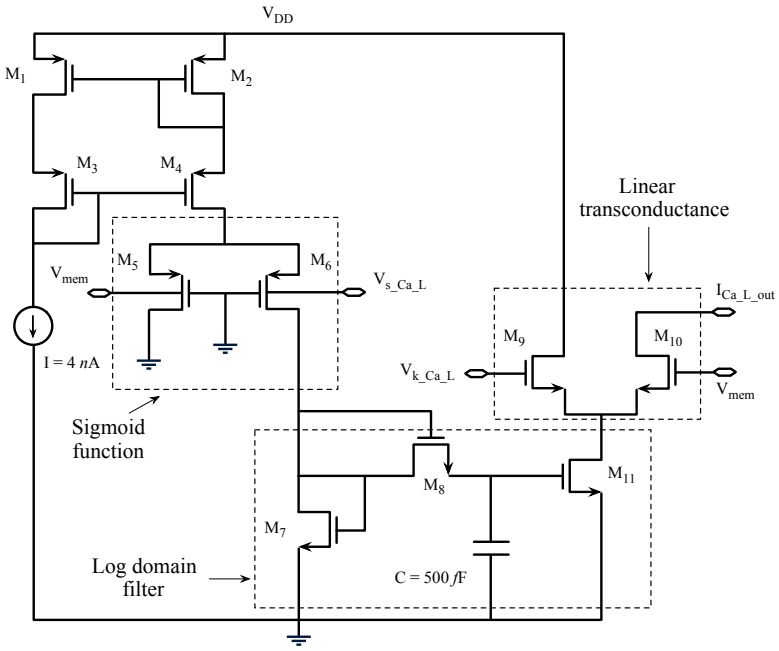

Figure 28: L-type Ca channel.

The L-type calcium current channel is shown in Fig. 28. In this design, the functional blocks are stacked on top of each-other to facilitate current reuse. A Wilson current mirror ($M_1 - M_4$) duplicates the current from the current source. The output current from M_4 is fed into a body driven sigmoid function block (M_5, M_6). $V_{s\_Ca\_L}$ serves as the reference voltage that controls the current steering point of the sigmoid function. The output current from M_6 in the sigmoid function block directly goes into the log-domain filter. In the log domain filter, M_7 acts as a nonlinear load and provides a low impedance for charging the capacitor C. The capacitor adds delay to the system. The delayed current from M_{11} in the log-domain filter acts as the bias current for the linear transconductor (M_9, M_{10}). The linear transconductor circuit is controlled by the gate voltages V_{mem} and $V_{k\_Ca\_L}$. The final output current $I_{Ca\_L\_out}$ is controlled by the voltage $V_{k\_Ca\_L}$ in the linear transconductor circuit. This current discharges the membrane capacitor through M_{10}.

The T-type calcium current channel is shown in Fig. 29. Similar to the Ca-L channel, the Ca-T channel consists of a Wilson current mirror that duplicates the current from the current source. The output current from M_4 flows into the sigmoid-function circuit. A

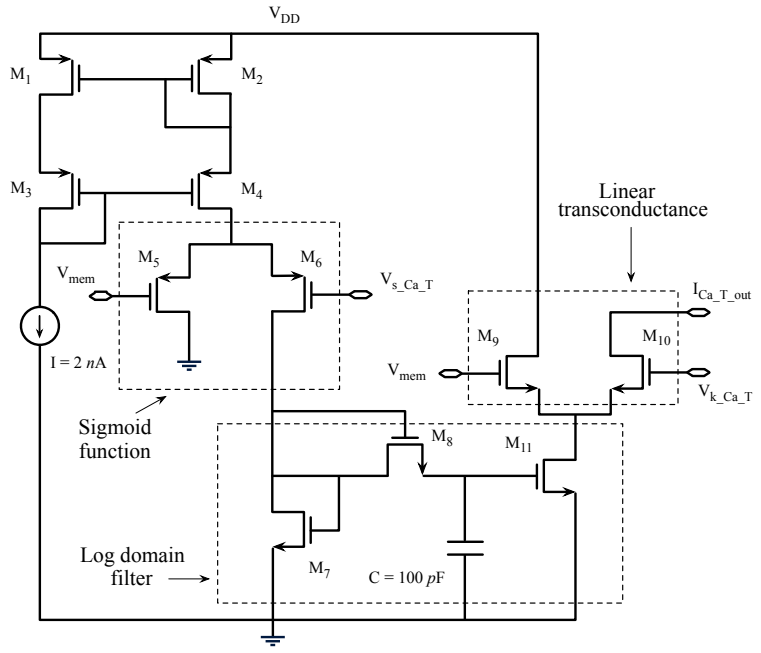

Figure 29: Circuit schematic of the T-type Ca channel.

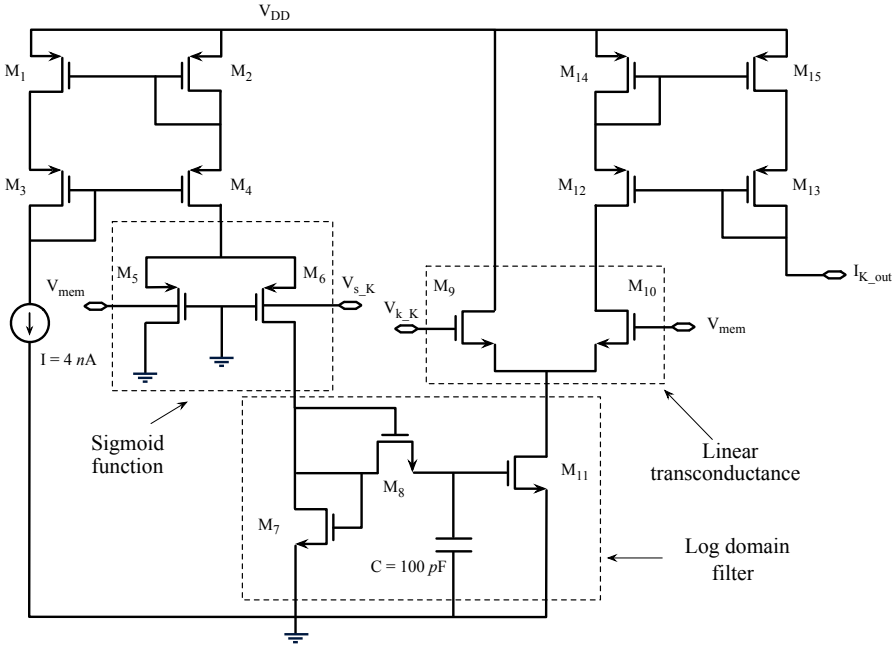

Figure 30: Circuit schematic of the Potassium (K) channel.

gate controlled sigmoid-function circuit is used in this channel, which results in the drain currents in M_5 and M_6 to have a faster response with the changes in V_{mem}. $V_{s\_Ca\_T}$ serves as the reference voltage that controls the current steering point of the sigmoid function. The output current from M_6 in the sigmoid-function circuit charges the capacitor C in the log-domain filter circuit(M_7, M_8, M_{11}, C). When V_{mem} is higher than $V_{k\_Ca\_T}$, the output current rapidly decreases for increasing V_{mem}. The final output current of the Ca-T channel, $I_{Ca\_T\_out}$, controlled by the voltage $V_{k\_Ca\_T}$, discharges the membrane capacitor.

The implementation of the potassium channel, shown in Fig. 30, is similar to the L-type calcium channel. The current reuse technique and the body controlled sigmoid function (M_5, M_6) have been used in this channel as well. A second Wilson current mirror ($M_{12}, M_{13}, M_{14}, M_{15}$) is employed at the output to duplicate the drain current in M_{10}. Unlike the L-type Ca channel current, the use of this current mirror results in the current, I_{K_out}, that charges the membrane capacitor.

The circuit schematic of the leakage channel is shown in Fig. 31. The leakage current represents the neuron current other than that contributed by the ionic current flow. This current has neither the non-linear behavior nor the differential coefficients present in the ionic currents. The schematic consist of a pair of current mirror and a linear transconductance. The final output current level controlled by the V_{K_L} port is directly fed into the membrane capacitor.

Simulation Results

The Si neuron cell is designed using 0.13 mm standard CMOS process. The channel width and the length of the MOSFETs used in the Ca-L, Ca-T, K and the leakage channels are 160 nm and 120 nm, respectively, with few exceptions. For the ion channels, the channel width and the length for M_7 are 320 nm and 120 nm, respectively. For the leakage channel, the MOSFETs M_5 and M_6 have channel width and length of 160 nm and 180 nm, respectively. The simulation results show that the system is capable of generating bursting and spiking signals based on the log domain filter's delay. The delay can be manipulated by changing

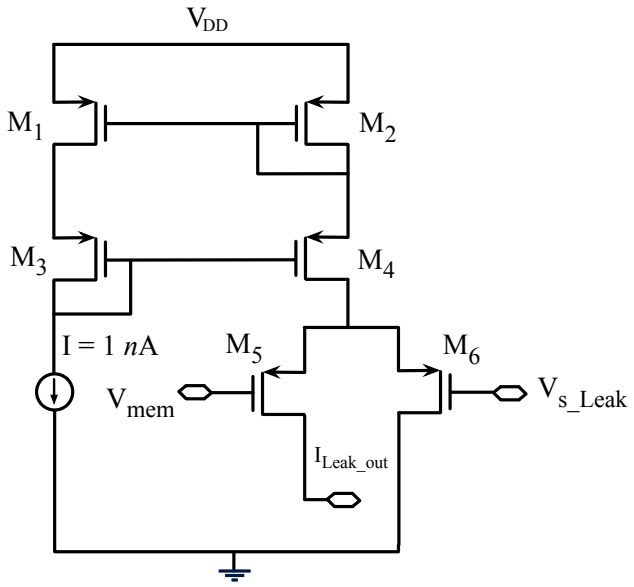

Figure 31: Circuit schematic of the leakage channel.

Table 3: Capacitor Values for the Log-Domain Filter and the Corresponding Neuron Output

	Spiking	Spiking Latency	Bursting	Chaotic
K Block Capacitor	0.3 - 0.33 pF	0.3 - 0.33 pF	100 - 300 pF	2-5 pF
Ca-T Block Capacitor	10 - 25 pF	26 - 120 pF	30 - 310 pF	0.8 - 1.2 pF
Ca-L Block Capacitor	0.9 - 1 pF	0.9 - 1 pF	0.1 - 2 pF	0.3 - 0.7 pF

the capacitor value in the log domain filter. Four distinct output signals were generated by the proposed design namely spiking, spiking latency, bursting, and chaotic signal. The range of capacitor values in the log domain filter for each ion-channel block for specific output type is shown in Table 3.

Initially, the capacitors in the log-domain filters in the Ca-L, Ca-T and K channels are in the range shown in the second column of Table 3. Such circuit configuration produces spiking output, which is shown in Fig. 32. When the membrane capacitor has very little charge, it is slowly charged by the leakage current. When the membrane capacitor potential reaches a specific value, the potassium channel opens, and the potassium channel current rapidly charges the membrane capacitor. The high potential in the membrane capacitor

results in current flowing through the Ca-L and the Ca-T channels, which discharge the membrane capacitor. Hence, the spiking output is observed. Spiking signal with amplitude 0.76 V, spiking width 10 *m*s, and frequency 43 Hz was observed.

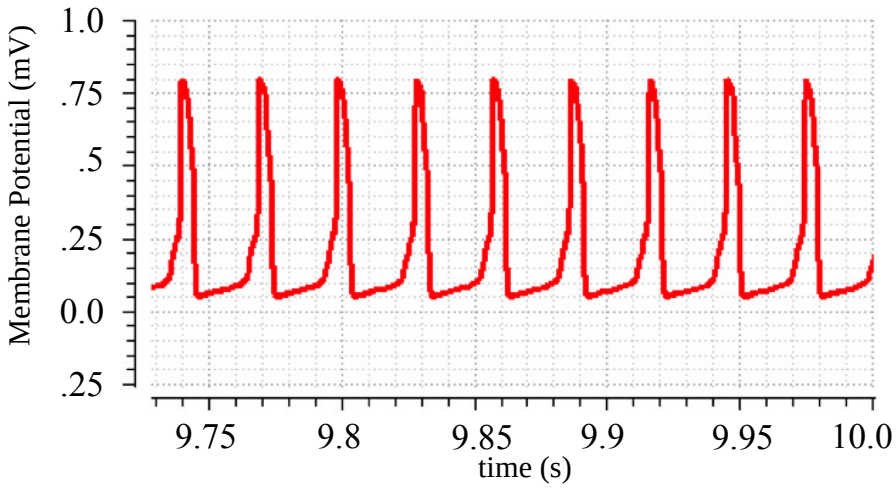

Figure 32: Tonic spiking output

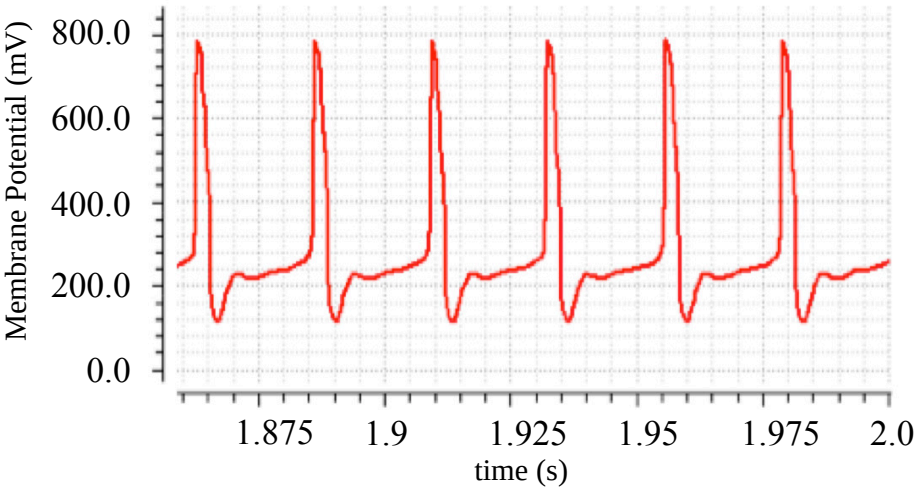

Figure 33: Spiking latency output

As the capacitor in the log domain filter in the Ca-T channel is changed within the range 26 - 120 *p*F, spiking latency output is observed, which is shown in Fig. 33. For the proposed

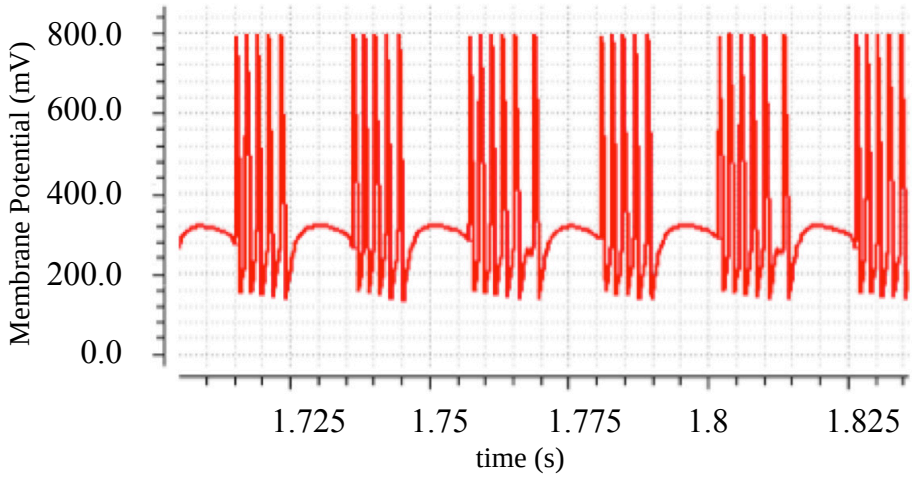

Figure 34: Bursting output

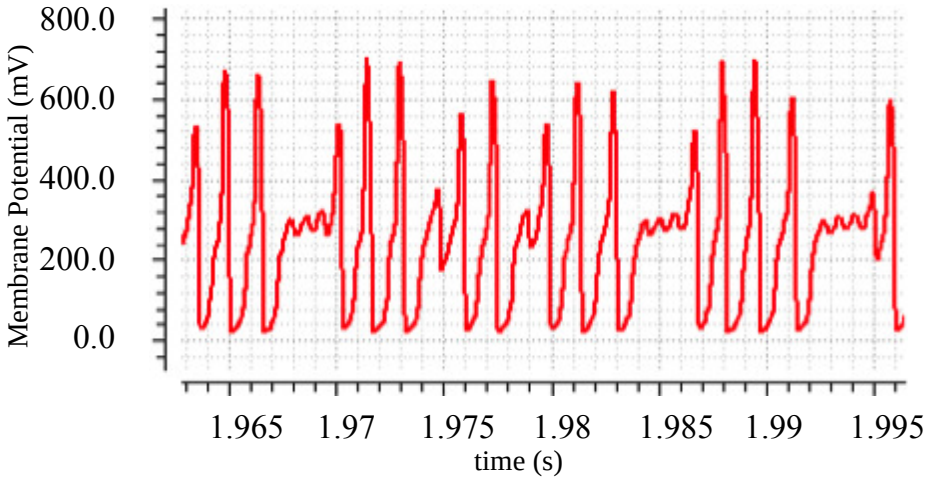

Figure 35: Chaotic output

circuit, spiking latency signal with an amplitude of 0.76 V, spiking width of 10 *m*s, and the signal frequency of 40 Hz was observed. Bursting signal, shown in Fig. 34, was observed as the third output of the proposed Si neuron. The bursting frequency of 400 Hz was observed, with 40 Hz bursting envelope and 0.76 V amplitude. The last variety of output generated by the proposed Si neuron is chaotic signal, which is shown in Fig. 35. The unbalance in the charging and the discharging current of the membrane capacitor results in chaotic output.

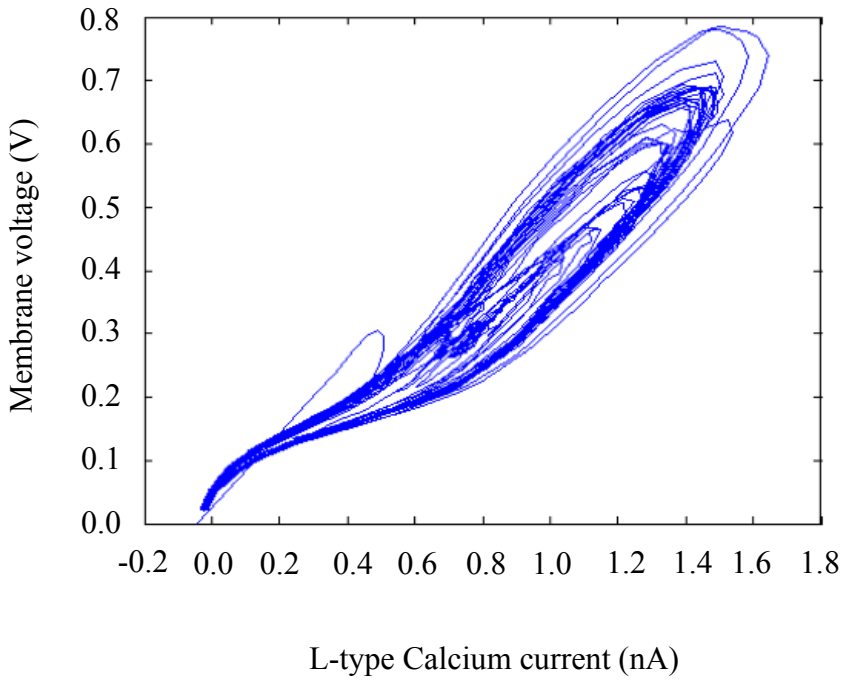

Figure 36: Phase-plane plot for L-type calcium current against membrane voltage.

Fig. 36 is the phase plane plot for membrane voltage versus L-type calcium current, which shows an attractor for a chaotic system. The chaotic behavior of the proposed Si neuron was confirmed by calculating the largest Lyapunov exponent (LLE). The L-type Ca current time series data from the proposed Si neuron circuit was used for the LLE calculation using the method explained in [**77**]. Fig. 37 shows the results of LLE calculation as a plot of log of divergence against time, for time series with 2000 data points. A positive LLE value of 1.83, obtained from the calculation, confirms that the fourth variety of signal produced by Si neuron circuit is chaotic.

A Monte Carlo simulation with 96% confidence factor is performed for the spiking output, which is shown in Fig. 38. For 80 iterations, the standard deviation is found to be 0.275 with the average frequency value of 12 Hz. The stability of the circuit performance meets the design requirement.

Table 4 shows the performance comparison of the proposed Si neuron architecture with the previously reported works.

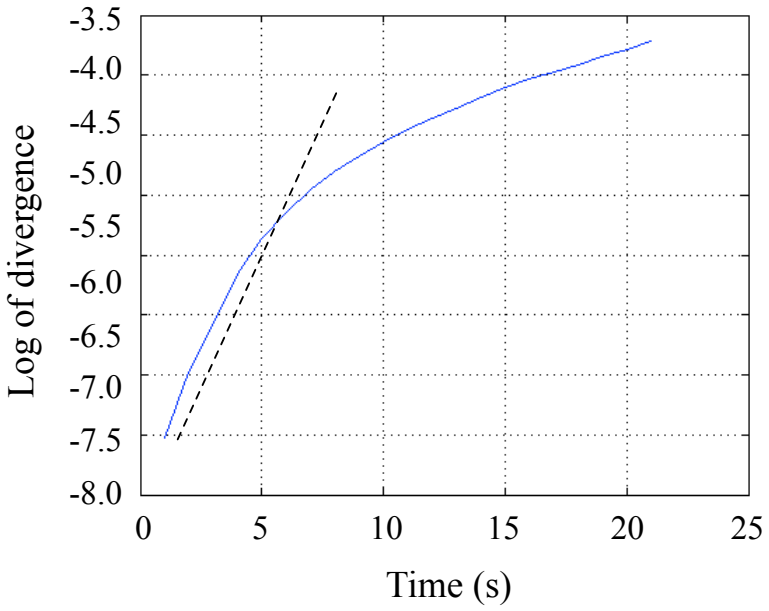

Figure 37: Plot of log of divergence versus time for LLE calculation. The slope of the dotted line gives the value of the largest Lyapunov exponent.

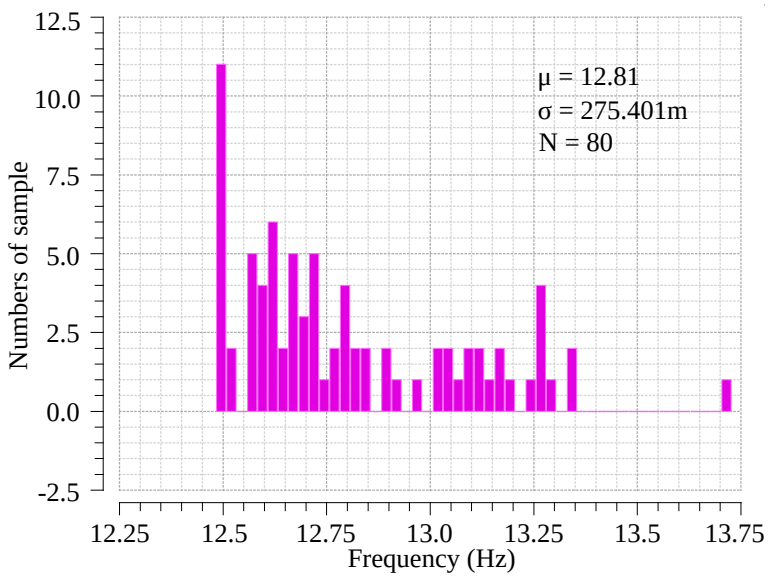

Figure 38: Monte Carlo simulation of spiking output.

Conclusion

A compact, ultra-low-power implementation of the bursting Hodgkin-Huxley model-based silicon neuron is presented in this paper. The proposed Si neuron is capable of generating

Table 4: Performance Comparison with Previously Reported Works

	[**71**]	[**72**]	[**78**]	This Work
Process	0.25 mm	1.2 mm	0.5 mm	0.13 mm
Supply Voltage	2.5 V	-	3.3 V	1 V
Power Consumption	4.5 mW	1 mW	300 mW	43 nW

four different outputs - spiking, spiking with latency, bursting, and chaotic signals. The different spiking outputs can be generated using the same circuit, by varying the value of the capacitor present in the log domain filter. Unlike conventional parallel structure for a log-domain filter, a simple structure has been adopted and stacked with the sigmoid function block for bias current reuse. The current reuse technique and subthreshold MOSFETs have facilitated ultra-low-power consumption. The compact Si neuron uses 43 MOSFETs. Simulation results show that the total power consumption, irrespective of the output signal type, is only 43 nW.

The silicon neural structure shows the ultra low-power. Furthermore the sigmoid block could generate gain, and log-domain low pass filter could generate the delay for the current. Those feature could be easily used in the filter or amplifier's circuit design.

Neuromorphic Bandpass Filter

We present a neuromorphic low-power bandpass filter [**79**]. The simplified Hodgkin Huxley neuron model is used in this bandpass filter design. Two current mirror based log-domain blocks working as sodium and potassium channels create the current sourcing and sinking profile. The center frequency can be tuned by the bias current. The proposed bandpass filter consumes only 5 nW with a 0.5 V supply for a center frequency of 200 Hz. The Monte Carlo simulation reveals 58 μV_{rms} input-referred noise and 1% THD for 7 mV_{p-p} of input signal. Our proposed structure achieves 41 dB dynamic range.

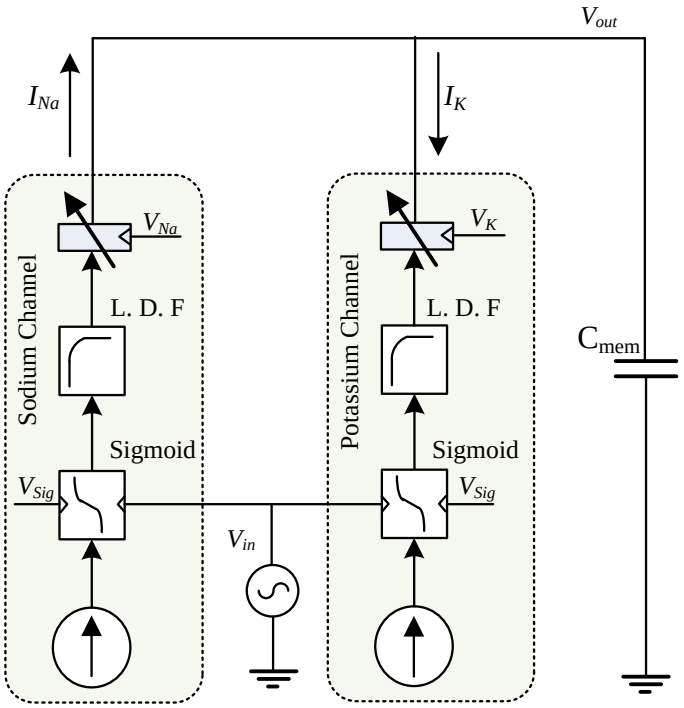

Figure 39: Block diagram of a neuron inspired bandpass filter.

The proposed neuromorphic band pass filter architecture is inspired by the ionic mechanism of the biological neuron. A single ion channel in the silicon neuron has three major blocks - sigmoid function block, log-domain block, and linear transconductor block [**1**]. The linear region of the sigmoid function can be used as the first gain stage of the operational amplifier. The current mirror based log-domain filter can add the delay into the current. The linear transconductor controls the final output current level. The the block diagram of the log-domain filter is shown in Fig. 39. A parallel connection of a potassium block and a sodium block in the filter achieves the sourcing and sinking mechanism. The output current from the sigmoid function feeds into the current mirror based log-domain filter. The capacitor in the log-domain filter adds the delay into the current and creates poles for the system. Finally, the current flows into a capacitor, C_{mem} through a linear transconductor circuit.

In order to save the power and reduce the noise contribution, the sigmoid block has been replaced by a subthreshold MOS based linear gain block. The linear transconductor block in the last stage of each channel has been removed to achieve higher gain. The circuit schematic of the proposed neuromorphic bandpass filter is shown in Fig. 40.

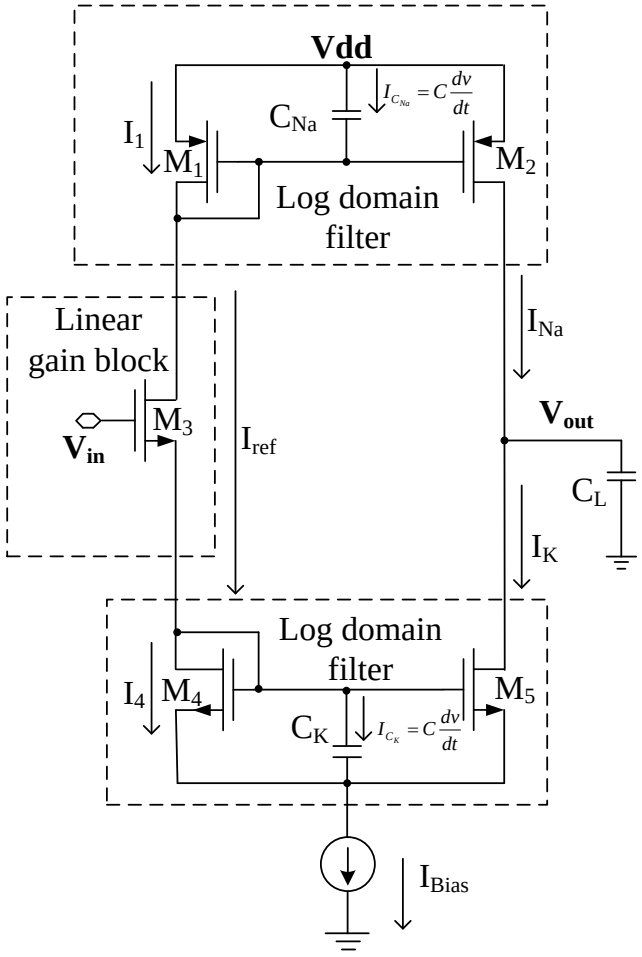

Figure 40: Circuit schematic of the proposed bandpass filter.

The input of the filter in Fig. 40 uses one NMOS for input signal. The total current flowing through the input transistor is controlled by the total bias current I_{Bias} and the input voltage V_{in}. The approximated linear expression of the current, I_{ref} is,

$$I_{ref} = \frac{I_0 \cdot I_{Bias} \cdot \kappa \cdot \left(\frac{W}{L}\right)_3 (1 + V_{in})}{U_T + \kappa I_{Bias}}, \tag{4.20}$$

where V_{in} is the input voltage, I_o is the technology current, $\kappa \approx 0.7$ is the non-ideality factor, and U_T represents the thermal voltage ($=\frac{kT}{q} \approx 25mV@27^oC$).

Frequency Response

The circuit can be divided into two different parts based on the charging current I_{Na} and the sinking current I_K. From Fig. 40, I_{Na} is the output of the top current mirror (M_1 and M_2) based log-domain filter. The capacitor in this block brings a pole into I_{Na}. The frequency response of the output current from the top section is,

$$I_{Na} = \frac{I_{ref} \cdot \frac{\kappa I_1}{C_{Na} \cdot U_T}}{s + \frac{\kappa I_1}{C_{Na} \cdot U_T}}, \tag{4.21}$$

where I_1 is the drain current flowing through M_1.

Similarly, the discharging current I_K can be expressed as

$$I_K = \frac{I_{ref} \cdot \frac{\kappa I_4}{C_K \cdot U_T}}{s + \frac{\kappa I_4}{C_K \cdot U_T}}, \tag{4.22}$$

Finally, the transfer function of the output voltage is,

$$\begin{aligned} &\frac{V_{out}}{V_{in}} = \beta \cdot \frac{s + \frac{\kappa(I_1 - I_4)}{U_T \cdot C_{Na} \cdot C_K (I_1 \cdot C_K - I_4 \cdot C_{Na})}}{\left(s + \frac{\kappa}{C_{Na} \cdot U_T}\right)\left(s + \frac{\kappa}{C_K \cdot U_T}\right)\left(s + \frac{r_2 + r_5}{C_L \cdot r_2 \cdot r_5}\right)} \\ &\textit{where} \\ &\beta = \frac{\kappa^2 \cdot I_0 \cdot I_{Bias} \left(\frac{W}{L}\right)_3}{U_T \cdot C_L \cdot C_{Na} \cdot C_K (I_1 \cdot C_K - I_4 \cdot C_{Na})(U_T + \kappa I_{Bias})}. \end{aligned} \tag{4.23}$$

Three poles and two zeroes are observed from the above equation. The pole locations are mainly controlled by the membrane capacitor, and the log-domain capacitors in each channel. The location of the first zero is controlled by the reference current, MOSFET transconductance, and log-domain capacitors. Due to the nano-ampere level reference current, the zero location is ahead of the first pole. The gain starts to increase by 20 dB/dec after the location of the zero. The first pole location gradually diminishes the gain increase resulting in a flat gain level and the second and the third poles lower the gain beyond the

higher cut-off frequency. The first pole is created due to the log-domain filter capacitor C_K in the potassium block. The second pole is created due to the capacitor C_{Na} which contributes the lower cut-off frequency. The output capacitor controls the location of the third pole.

Simulation Results

The proposed low-power neuromorphic bandpass filter has been designed in 0.13-μm standard CMOS technology. The entire filter structure consists of 5 transistors. The neuron-inspired structure and sub-threshold MOSFETs have been used to achieve low-power consumption. The charging and discharging profiles of different ionic channels of a Si neuron are utilized to achieve the bandpass filter characteristics.

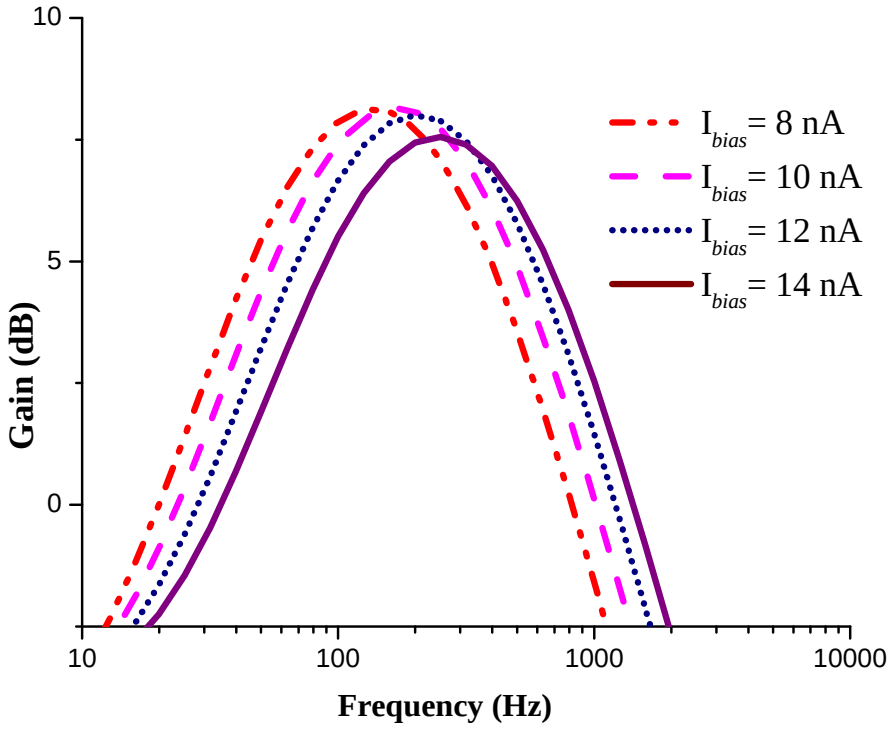

Figure 41: Magnitude response of the proposed bandpass filter.

The magnitude of the frequency response is shown in Fig. 41. The center frequency moves almost linearly for 150 Hz to 300 Hz of the proposed bandpass filter for the reference current I_{Bias} ranging from 5 nA to 15 nA.

Fig. 42 shows the Monte Carlo simulation results of the integrated input-referred noise due to the device mismatch and process variation. An average input-referred noise voltage of 58 μV_{rms} is obtained with a standard deviation, σ of 14×10^{-6} V. A transient simulation with a sinusoidal input of 7 mV_{p-p} and 200 Hz frequency, is performed. The corresponding Monte Carlo simulation as shown in Fig. 43 depicts a total harmonic distortion of 1.3% with a σ of 0.9.

With a 0.5 V supply and for a center frequency of 200 Hz, the power consumption of this bandpass filter is 5 nW. According to the THD and input-referred noise results from the Monte Carlo simulation, the dynamic range of the proposed architecture is 41 dB.

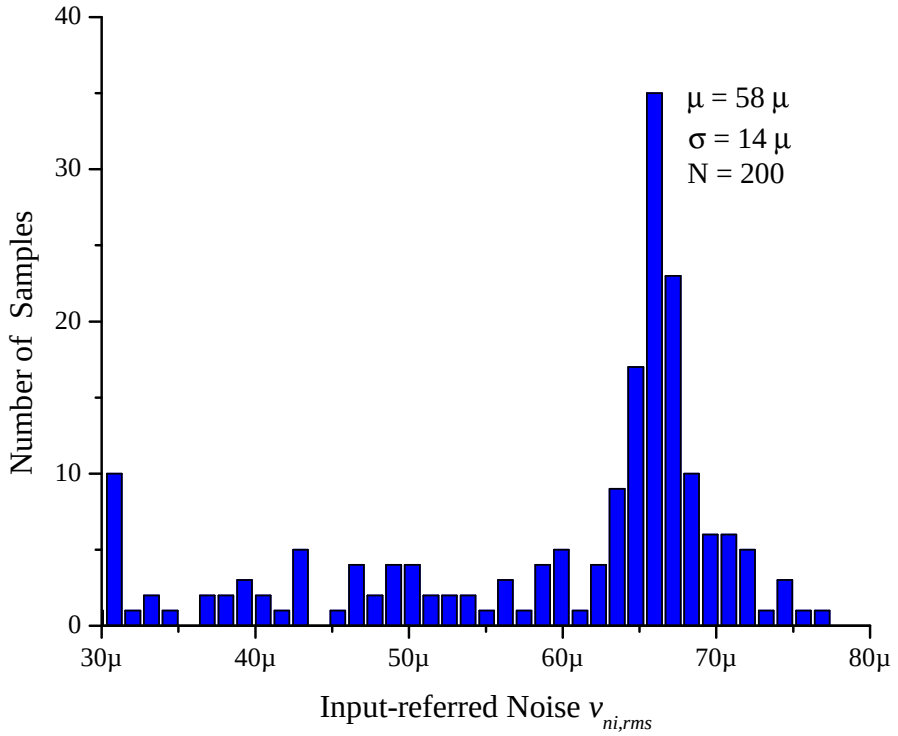

Figure 42: Monte Carlo of the input-referred noise.

Conclusion of neuromorphic bandpass filter

In this paper a neuromorphic ultra-low-power bandpass filter is presented. The current sourcing and sinking profiles of different ionic channels in silicon neuron are utilized to

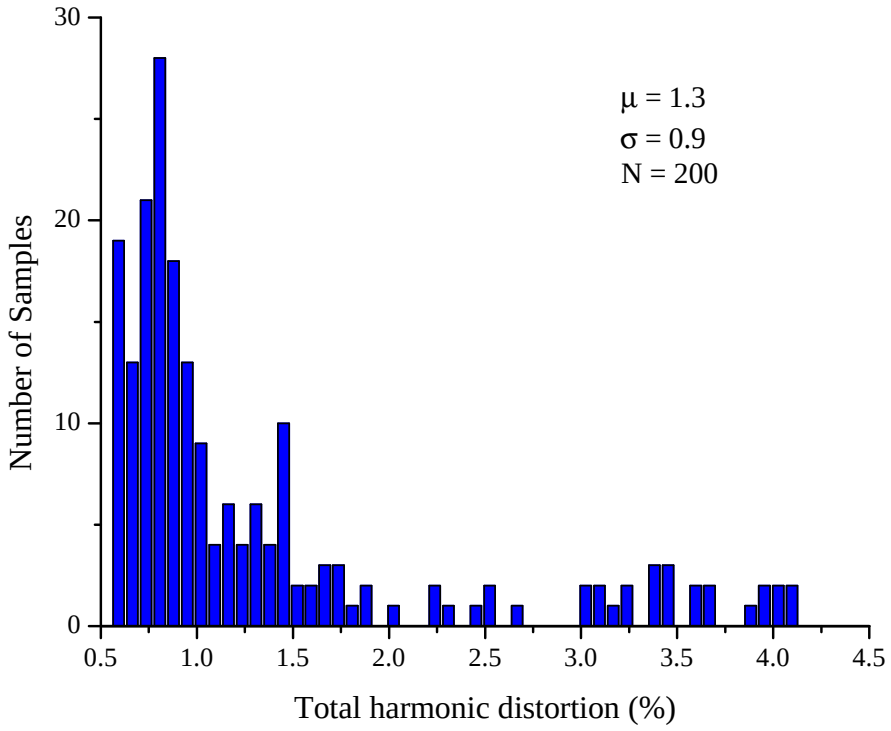

Figure 43: Monte Carlo of the THD (%) with 7 mV_{p-p} input voltage.

achieve the bandpass filter characteristics. The filter is designed in a standard 0.13-μm CMOS process with only 5 transistors working in the weak-inversion saturation regions. The proposed bandpass filter consumes 5 nW with a 0.5 V supply for a center frequency of 200 Hz. The center frequency can be tuned from 150 Hz to 1.5 KHz. The Monte Carlo simulation reveals 58 μV_{rms} input-referred noise and 1% THD for 7 mV_{p-p} of input signal, that results in a dynamic range of 41 dB.

Bioinspired Bandpass Biopotential Amplifier-Filter Bank

The proposed amplifier-filter mimics the ionic current flow mechanism of the neuron. The current sourcing and sinking profiles of sodium and potassium channels in silicon neuron are utilized to achieve the amplification and bandpass characteristics. The design is focused on the narrow band in each channel to improve the input-referred rms noise performance and noise-efficiency factor (NEF). By selecting the certain frequency band for each channel,

the amplifier-filter bank could cover the entire frequency spectrum. The amplifier-filter bank consumes a total of 1.8525 μW for the signal band of 40 Hz to 10.8 KHz and shows noise-efficiency factor of approximately 3 per channel.

System Architecture

The block diagram of the proposed amplifier-filter bank is shown in Fig. 44. Four amplifier-filter blocks are connected in parallel to a common electrode. The higher-cutoff frequency of the preceding block coincides with the lower-cutoff frequency of the succeeding block. By combining four blocks, the amplifier-filter covers the frequency range from 40 Hz to 10.8 KHz. The distributed band coverage topology achieves low-noise, low NEF and ultra-low-power consumption.

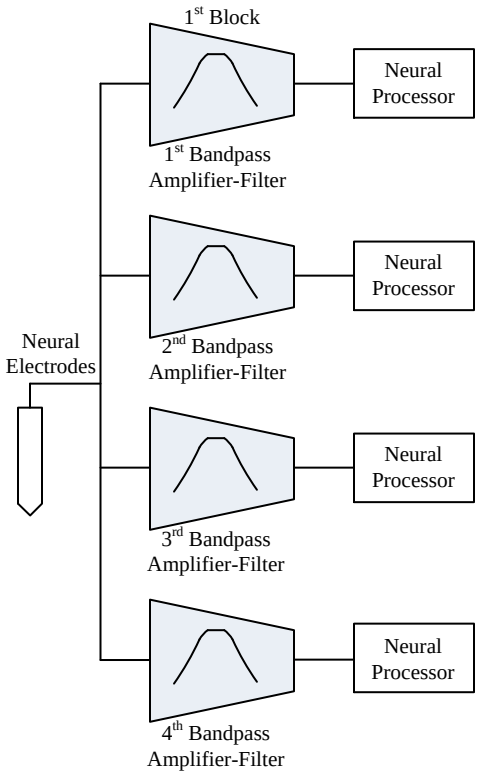

Figure 44: Block diagram of a neuron inspired amplifier-Filter bank.

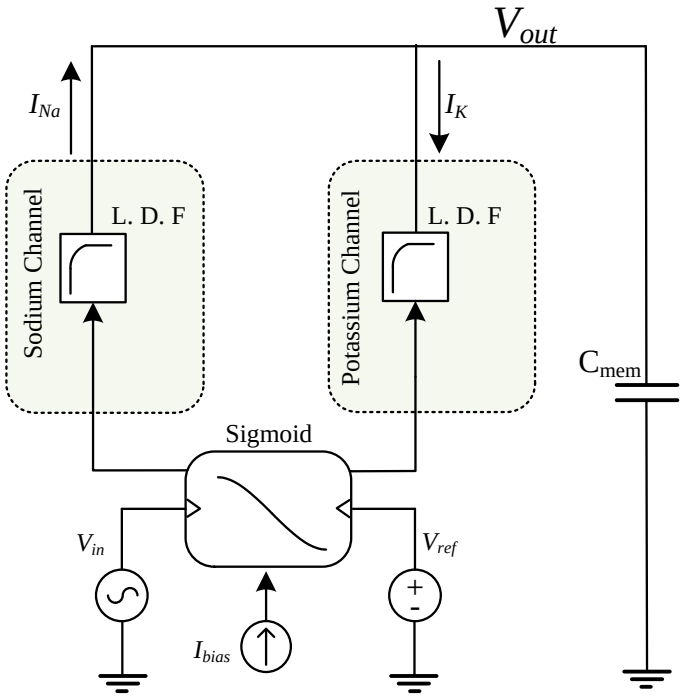

Figure 45: Block diagram of a neuron inspired amplifier-filter.

The block diagram of a neuromorphic amplifier-filter is shown in Fig. 45. The simplified Hodgkin Huxley neuron model uses two current mirror based log-domain blocks to form the sodium and potassium channels. The action potential is created by sourcing and sinking current through sodium and potassium channels. The individual ion channel of the silicon neuron contains three major blocks - sigmoid function block, log-domain block, and linear transconductor block [**1**]. The linear region of the sigmoid function is used to create the first gain stage of the operational amplifier. A series connection of a potassium block and a sodium block in the filter achieves the sourcing and sinking mechanism. The output current from the sigmoid function is fed into the current mirror based log-domain filter. The capacitor in the log-domain filter adds delay to the current and creates poles for the system. Finally, the resultant current from the sodium and potassium channels flows into a capacitor C_{mem} through the linear transconductor block.

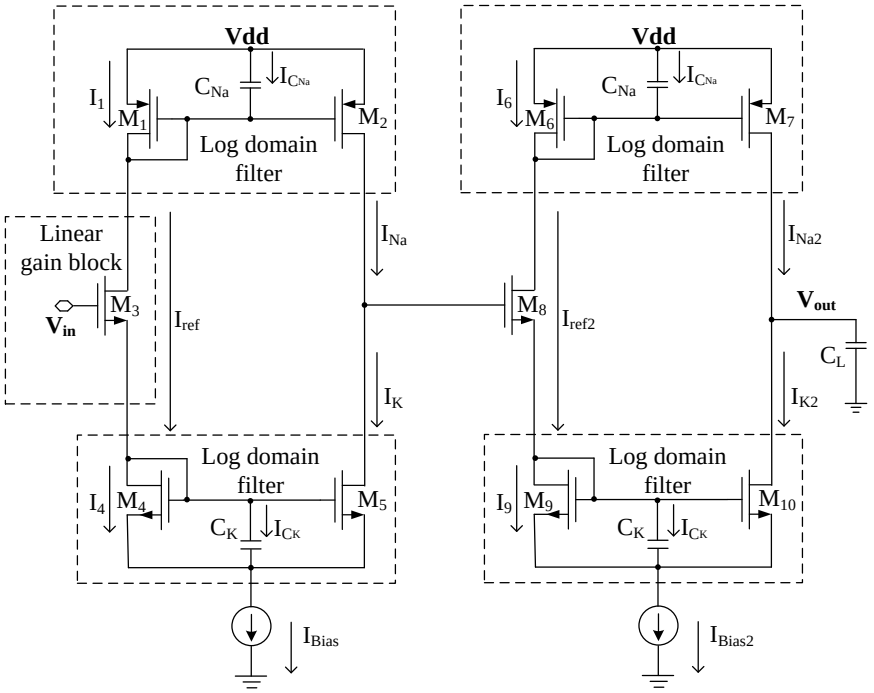

Figure 46: The schematic of a single biopotential bandpass amplifier-filter.

In terms of the power saving and the noise reduction, the sigmoid block has been replaced by a subthreshold MOS based linear gain block. The PMOS based log-domain filter creates the time constant of the sodium current, and the NMOS based log-domian filter creates the time constant of the potassium current. The linear transconductor block has been removed to achieve high gain [**80**]. Two opposite currents with different delay constants make the system behaving as a bandpass filter. The circuit schematic of the proposed amplifier-filter is shown in Fig. 46. By cascading two similar blocks, the amplifier-filter shows higher gain and sharper bandwidth.

Simulation Results

The proposed amplifier-filter bank has been designed in 0.13-μm standard CMOS technology. The neuron inspired architecture and distributed filter bank principle have been used to achieve low-noise and low NEF with ultra-low-power consumption. Fig. 47 is the gain plots

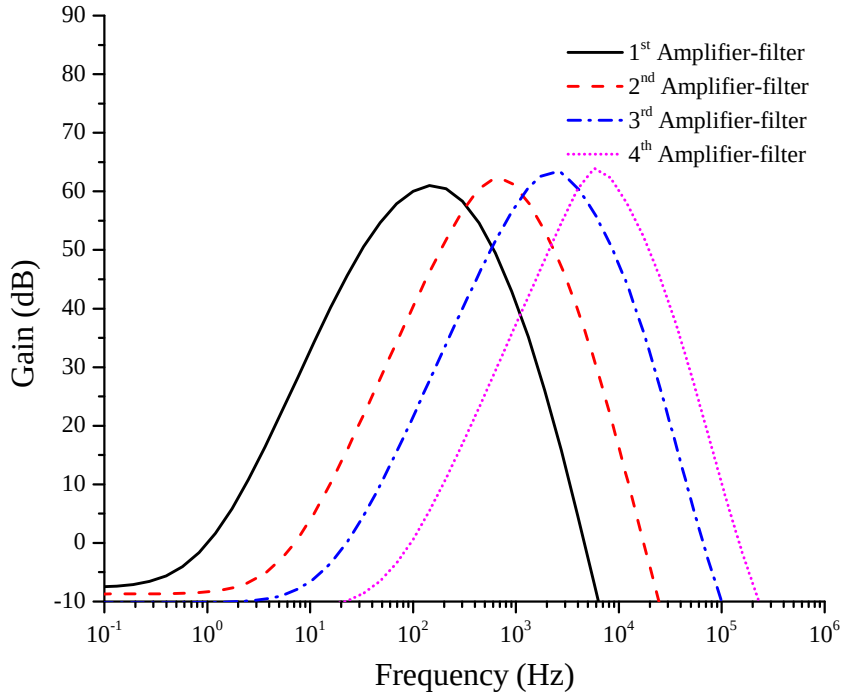

Figure 47: The gain plots of the biopotential bandpass amplifier-filters.

Table 5: Performance summary of the proposed biopotential bandpass amplifier-filter bank

	1^{st} block	2^{nd} block	3^{rd} block	4^{th} block
Bandwidth (Hz)	360	1000	2800	6600
Lower-cut off frequency (Hz)	40	400	1400	4200
Higher-cutoff frequency (Hz)	400	1400	4200	10800
Input-referred noise (μV_{rms})	10	8.8	6.8	6.9
NEF	2.4	3.1	3.2	2.9
Power (μW)	0.015	0.0825	0.465	1.29
Max. signal (1% THD) (μV_{p-p})	80	240	200	230

of each amplifier-filter with center frequencies at 200 Hz, 900 Hz, 2400 Hz, and 7700 Hz. In order to cover the entire biosignal frequency band, the higher-cutoff frequency of the preceding block coincides with the lower-cutoff frequency of the succeeding block. The results showed that the amplified-filter bank not only precisely selects the desired sub-band but also amplifies the signal. Fig. 48 shows the individual input-referred noise of the amplifier-filter blocks. The resultant bandwidth allocation among all the amplifier-filter blocks shows an exponential behavior as shown in Fig. 49.

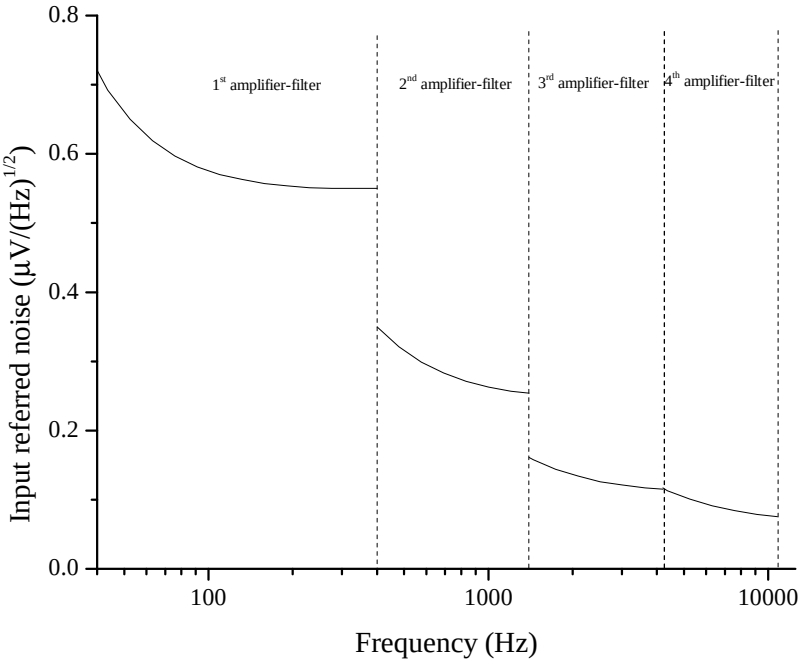

Figure 48: The input-referred rms noise of each amplifier-filter block.

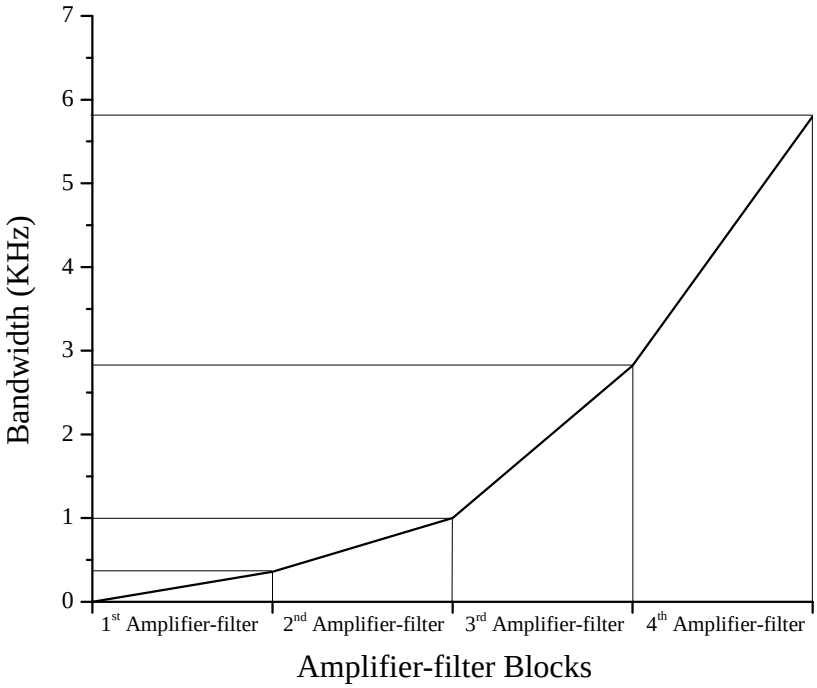

Figure 49: The bandwidth allocation among all the bandpass amplifier-filters shows the exponential increase.

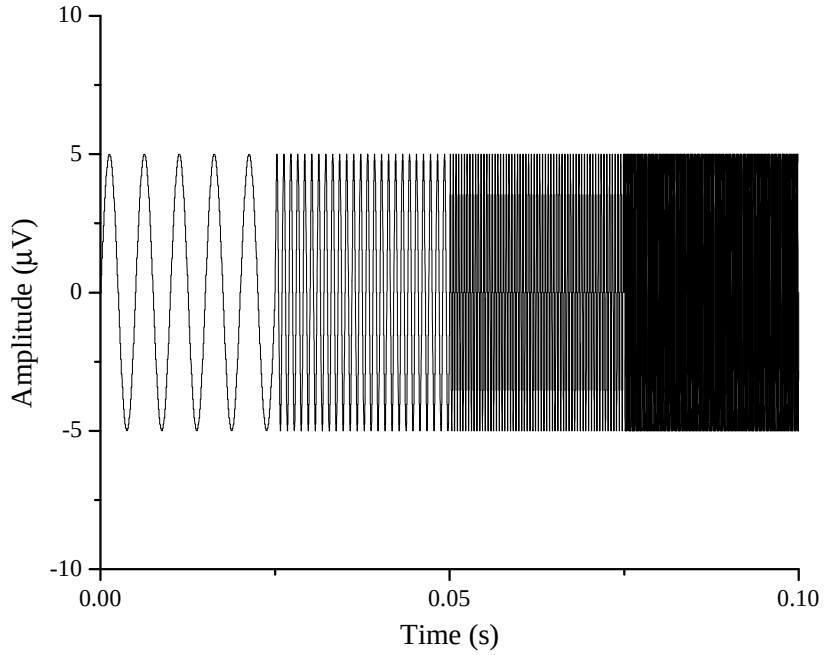

Figure 50: The input synthetic sinusoid signal with frequency components of 300 Hz, 1000 Hz, 3000 Hz, and 6000 Hz.

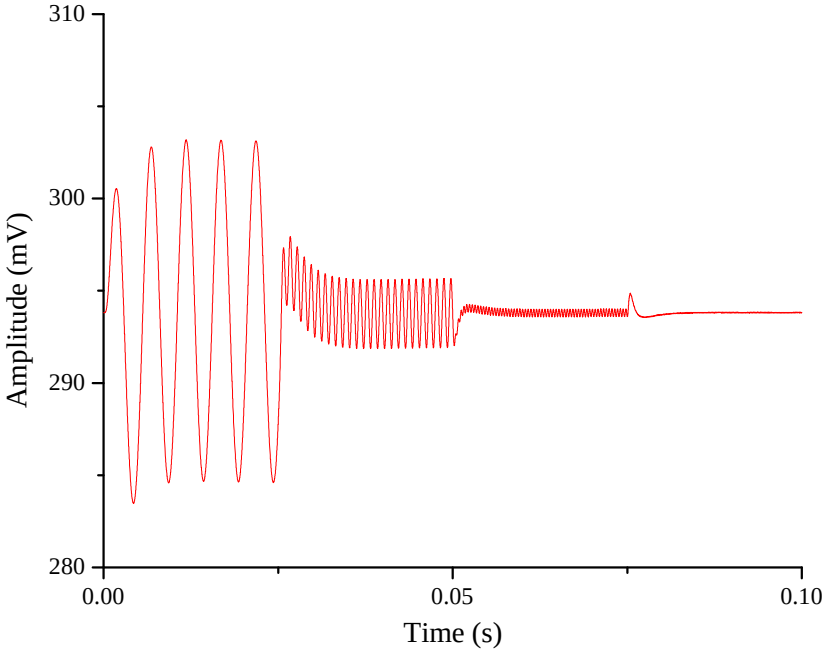

Figure 51: The output results of the synthetic sinusoid signal form the fist block.

Table I shows the performance summary of all the amplifier-filter blocks in the bank. The input-referred rms noise is less than 10 μV_{rms} for most of the blocks and the highest NEF is

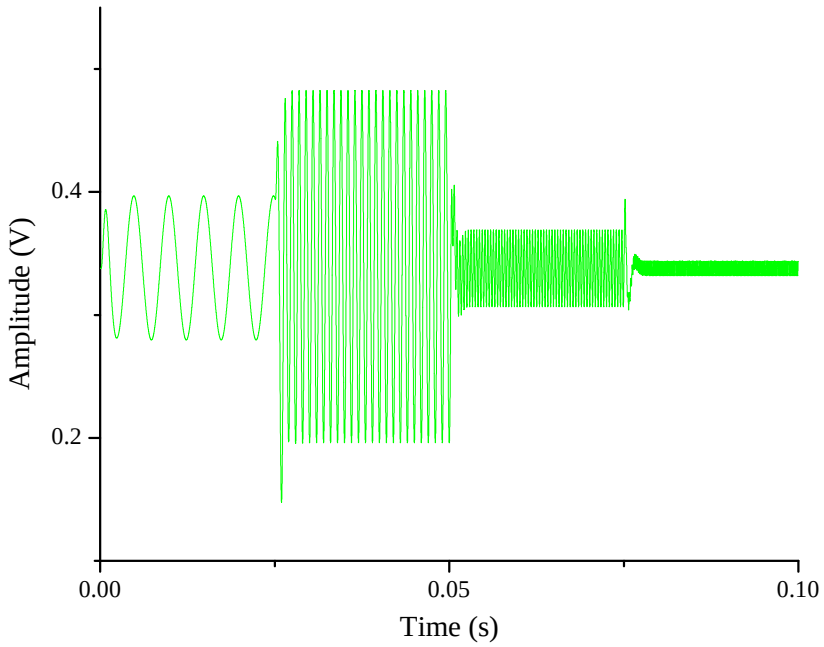

Figure 52: The output results of the synthetic sinusoid signal form the second block.

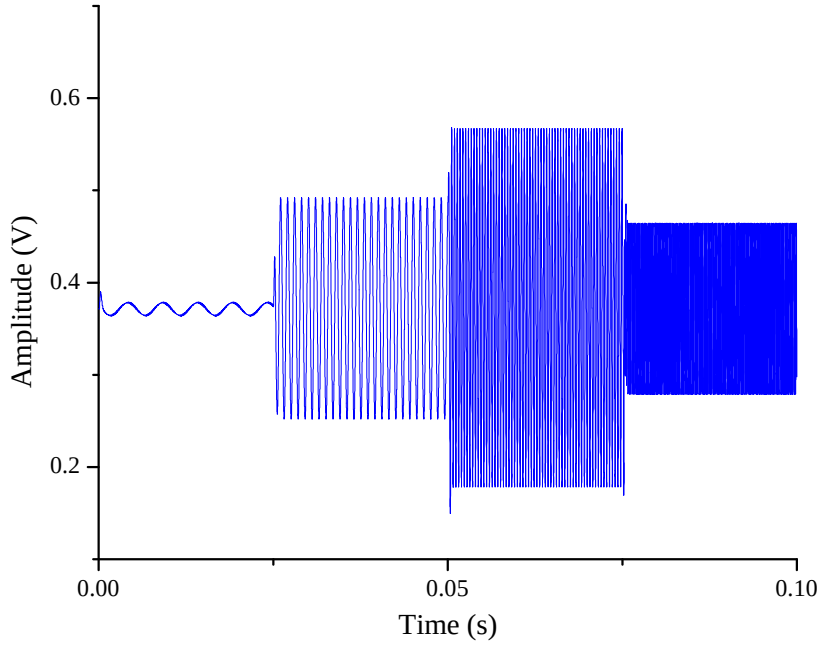

Figure 53: The output results of the synthetic sinusoid signal form the third block.

only 3.2. The total power consumption of the entire amplifier-filter bank is only 1.8525 μW. Comparing to the conventional biopotential amplifier, the proposed amplifier-filter bank significantly decreases the power consumption with minimum compromise with the system

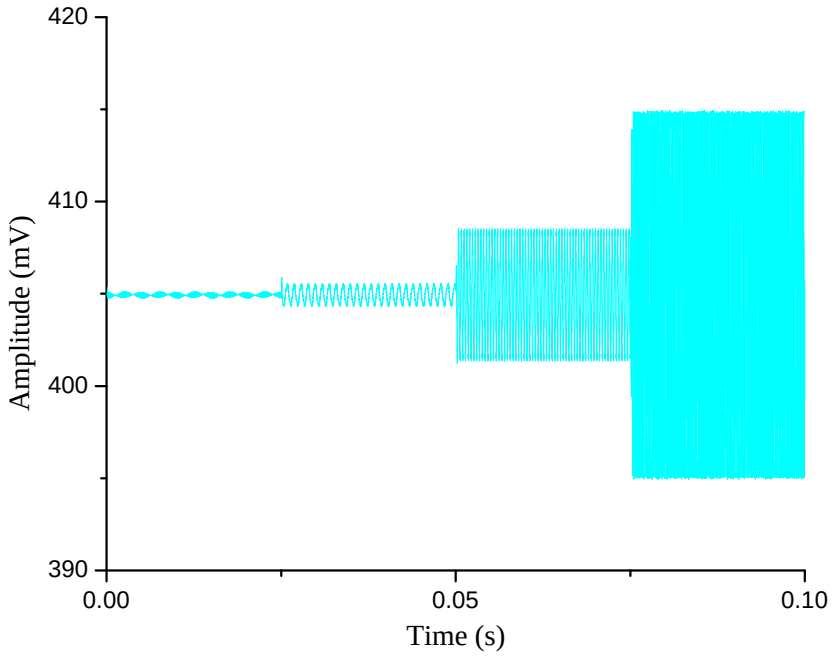

Figure 54: The output results of the synthetic sinusoid signal form the forth block.

performance. Fig. 50 is the synthesized input sinusoid signal with frequency components of 300 Hz, 1000 Hz, 3000 Hz, and 6000 Hz. As is shown in Fig. 51, the high frequency component is precisely filtered out by the first block in the amplifier-filter bank. Fig. 54 is the output of the fourth amplifier-filter block corresponding to the synthetic sinusoid input signal.

Layout and post-layout simulation

In order to verify the circuit performance, the layout has been drawn by Cadence layout tools. The layout of the amplifier filter bank includes four blocks with same structure as showed in Fig.55. The different value of the capacitors had been used to control the low and high cut off frequency. Over 90% of the chip area is occupied by capacitors. Due to the low frequency coverage, the capacitor size must be large enough. From the layout figure we can find that the the first amplifier filter block constants the largest capacitor. By the increase of the center frequency of the amplifier filter block, the size of the capacitor deceases. The forth

amplifier filter block which has a highest center frequency has smaller capacitors compared to the first block.

Same as the schematic, all blocks' input pins are connected together. The output pins of each amplifier filter block are separated. The system is biased different bias current with individual bias current source. The post layout simulation of proposed amplifier filter band is shown in Fig. 56. The post layout simulation has the same amplitude of the schematic simulation. The forth filter's amplitude is silty low than the schematic is because of the parasitic capacitors from the output pad and thick metal line. In order to increase the signal band in the low frequency rang,I have use the large capacitor for the first block. The lowest frequency reaches to 1.5Hz.

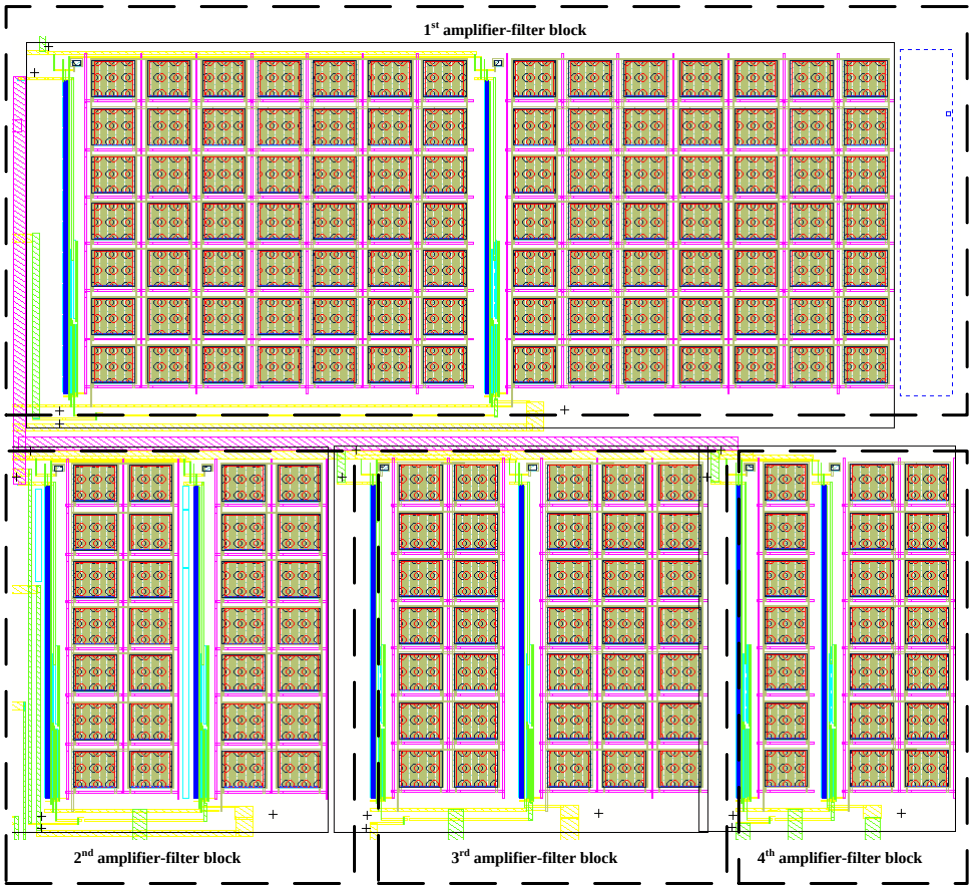

Figure 55: The layout of proposed amplifier-filter bank

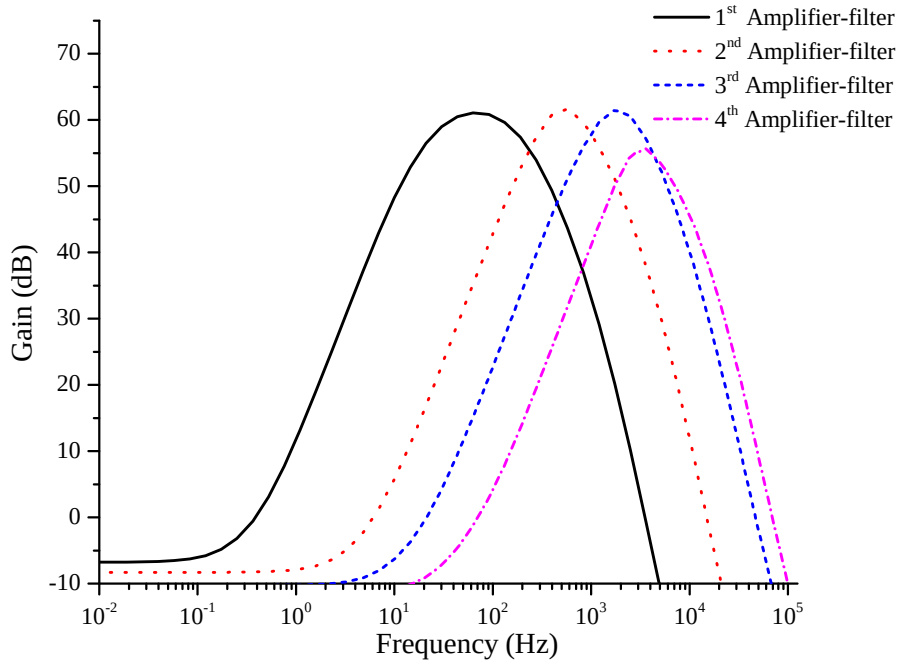

Figure 56: The frequency response of the post-layout simulation of the proposed amplifier-filter bank

Conclusion of amplifier-filter bank

In this paper a distributed amplifier-filter bank with excellent NEF and power consumption is presented. The circuit achieves the bandpass and amplification characteristics by mimicking the current sourcing and sinking profiles of the neuron. The high gain output and sharper bandwidth is contributed by cascade connection of two similar blocks. Multi-channel architecture of the proposed system provides the amplification and frequency selective signal inspection without the need of high bandwidth amplifier and a separate filter bank. Considering the typical input-referred noise profile, smaller bandwidths are allocated near the flicker noise zone and wider frequency bandwidths are allocated for the thermal noise zone. The proposed amplifier-filter bank is designed in 0.13-μm standard CMOS process and the resultant structure consumes a total of 1.8525 μW with 1 V supply voltage. The system contains four amplifier-filter bank with the signal band coverage of 40 Hz to 10.8 KHz and shows NEF of approximately 3 per channel. The parasitic capacitors from the pad and thick metal line benefits the lower cut off frequency of the first block. The proposed

amplifier-filter provides the better solution of the amplifier and filter stages of implantable system in terms of power consumption and noise performance.

A Low-Power Silicon Neuron Based Biopotential Amplifier

In recent neuroscience research demands for more accurate and reliable biopotential signals from the neuron synapses. A high resolution implantable biopotential recording system has the ability of capturing the detail information of the vital physiological phenomena in the biosignal. The ultra-low-power implantable device with *in situ* sensor can minimize the skin irritation from the frequent operations for battery replacement. In emerging clinical applications including brain rehabilitation and epilepsy treatment, a implantable device shows great promise [**2**].

An implantable biopotential recording system usually includes a powering unit, a signal processing unit, a data conversion unit, and a wireless communication unit. [**60**][**59**]. The bio-electrical signal from the active neuron is captured by an implantable sensor, the data acquisition unit in the biopotential recording system. A bioamplifier, one of the critical components of the implantable neural recording system, is then used to suppress the low frequency noise and amplify the different types of bio-signals depending upon the applications. Electrocardiography (ECG), Electroencephalography (EEG), Electromyography (EMG), and Electrooculography (EOG) are the commonly used biosignals from the implantable electrodes that are utilized for further data processing.

The biopotential amplifies are specifically designed for bio-signal with the common features of low frequency, and low amplitude level. ECG signals are in the range of 0.01 Hz - 300 Hz with the amplitude range of 0.05 mV - 3 mV, EEG signals are in the range of 0.01 Hz - 100 Hz with the amplitude from 1 μV to 1 mV, EOG signals are in the rang of 0.1 Hz - 10 Hz with the amplitude from 1 μV to 300 μV, and EMG signals, which have the highest frequency, are in the range of 50 Hz - 3000 Hz with the amplitude from 50 μV to 100 mV. The amplitude of a biosignal ranges from 50 μV- 500 μV with the noise level of 5 μV - 10μV. The input-referred noise of the biopotential amplifier should be below the 10

μV which comes from the background noise of the electrode. The power dissipation should be below 100 μW per channel in a multichannel system to reduce the risk of necrosis in the tissue by heating [**34**][**81**]. To cover the frequency range of all types of biosignals, the desired frequency bandwidth could be below 10 KHz [**34**].

The electrode offset-potential coming from the electrode-tissue interface can easily saturate the output stages to limit the amplifiers' admissible gains [**82**], thus the conventional low-pass amplifiers are usually not suitable for DC-coupled biopotential signals. The biopotential amplifiers with low frequency suppression technique can filter out the DC offset from the electrode in order to increase the input signal range. In the recent biopoential amplifier design area, two major low frequency suppression methods have been used: passive low frequency suppression by using serial blocking capacitor and active circuits based on closed-loop control of the DC level [**83**]-[**87**].

A passive serial blocking capacitors require an additional high-pass filter at the amplifiers' input stage in order to remove the offset voltage from the sensor electrode. However, due to the bias resistors, the input signal from the RC coupling network is becoming lower and the offset voltage of the amplifier is getting higher. [**82**]. Furthermore, the capacitance variation from the tissue and the surface of the probe is directly co-effected with the input RC high pass filter. The lower cut-off frequency and the input amplitude are directly affected with the variation of capacitance from the tissue.

The low frequency suppression techniques of rejecting DC input voltage from the electrode by using DC negative feedback from the output terminal, can not only avoid the mismatch from the passive input devices, but also decrease the input-referred noise as well as the total impedance of the circuit [**88**]. However, this technique needs large integrated capacitors in order to maintain the high gain. The active low frequency suppression with the miller capacitor can overcome the capacitor size concern of the conventional low frequency suppression techniques. To reduce the capacitor size, the active schemes based on closed loop control of DC levels are reported in [**88**]-[**90**].

In this work, we propose a low-power bio-inspired Hodgkin Huxley(H-H) silicon neuron based biopotential amplifier with active low frequency suppression. The H-H model is a neuromimetic design that provides the most accurate representation of the ionic dynamics [**73**]. It models the Si neuron based on the ionic flow through the neuron membrane with a set of equations. The basic H-H model consists of two current channels, a potassium current channel for current sinking and a sodium current channel for current sourcing [**73**]. By the combination of the two delayed currents from the sodium and the potassium channels, the system performs the bandpass characteristic. The lower cut-off and the higher cut-off frequencies are controlled by the internal capacitors other than the capacitor from the input stage, thus the proposed biopotential amplifier is insensitive to the capacitance variation from the electrode or tissue.

This paper presents the design and performance of a new bio-inspired silicon neuron based biopotential amplifier that achieves active low-frequency suppression. The transfer function of the proposed amplifier shows that the low frequency suppression is achieved by the locations of the tunable zeroes and poles. The proposed biopotential amplifier can offer a gain of 34 dB with a -3 dB bandwidth of 7.2 KHz. The amplifier is designed in a 0.13 μm standard CMOS process and the total power consumption of the core part with 500 mV supply voltage is 4.4 μW. The input-referred noise is 6.9 μV_{rms} integrated over the entire band with a noise efficiency factor (NEF) of 9.2.

Architecture of the Biopotential Amplifier

The ionic current flow mechanism of the silicon neuron has been used in the biopotential amplifier design. In the silicon neuron, the action potential is created by the alternate charging and discharging of the membrane capacitor. Fig. 57 shows the transient plot of the action potential of a silicon neuron corresponding to the sodium and the potassium currents. The sodium current charges the membrane capacitor when the adjacent membrane voltage is high. The potassium current discharges the same membrane capacitor until the membrane voltage reaches the threshold level.

The input signal from the membrane opens up the voltage sensitive sodium channel and thus the sodium current, working as a current source, charges the membrane capacitor. After a short delay, the potassium channel starts to sink the current from the membrane capacitor. The membrane capacitor converts those two delayed currents into the action potential which is shown in the bottom plot of Fig. 57.

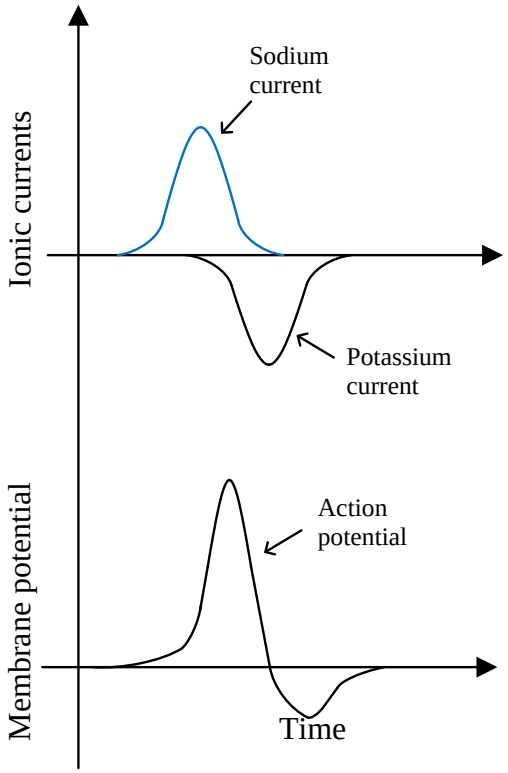

Figure 57: The top plot shows the time domain ionic current flow in ideal case [**1**]. The sodium current, working as a current source, charges the membrane capacitor at the beginning. After a short delay, the potassium current starts to sink the current from the membrane capacitor. The membrane capacitor converts those two delayed currents into the action potential voltage that is showed at the bottom.

The autonomous silicon neuron with four channels has been reported in [**1**]. The block diagram of the prototype is shown in Fig. 58. Each channel is implemented by a sigmoid-function block, a log-domain filter, and a linear transconductor. The linear region of the sigmoid-function is used in the amplifier design. The delay current is generated by sodium currents by the log-domain filters. A linear transconductor controls the output current directions. The potassium block and the sodium block are connected in parallel to a capacitor. The bias current passes through the sigmoid function which is controlled by a reference voltage V_{ref}. The capacitors in the log-domain filters add the delays into the current from the sigmoid block and create poles. Finally, the two currents with different delay and opposite polarity flow into the membrane capacitor, C_{mem}, to create the output voltage.

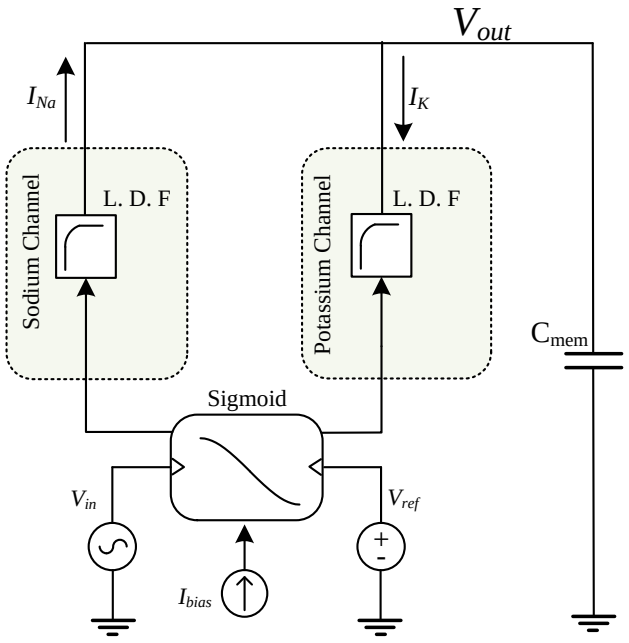

Figure 58: The block diagram of the proposed biopotential amplifier. L.D.F stands for log-domain filter. The sigmoid function, controlled by the reference voltage, provides the gain of the amplifier.

Fig. 59 shows the functional block diagram of the transfer function of the proposed biopotential amplifier. The input signal $R(s)$ is amplified by the gain blocks $G_{Na}(s)$ and $G_K(s_)$. Different delay $\tau_{D_{Na}}$ and τ_{D_K} are added by log-domain filters $H_{Na}(s)$ and $H_k(s)$, respectively. The output $O(s)$ is the combination of those two delayed function. In the following the transfer function of the ideal behaviour of the proposed neuron-inspired amplifier is presented with the help of superposition principle.

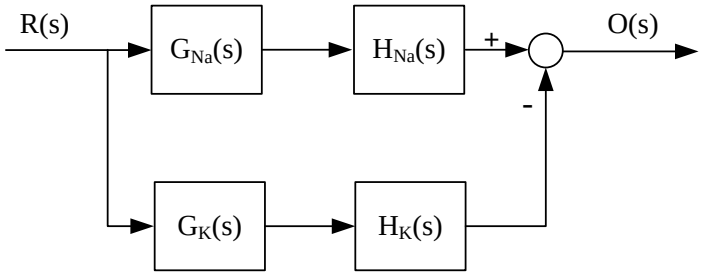

Figure 59: Equivalent system for the transfer function of the silicon neuron based biopotential amplifier, with input $R(s)$, gain $G(s_{Na})$ $G(s_K)$, delay $H(s)$, and output $O(s)$.

The transfer function when the potassium channel is inactive,

$$\frac{V_{out_{Na}}}{V_{in}}(s) = \frac{A_{v_{Na}(s)}}{(s+\tau_{Na})(s+\tau_{out})}. \tag{4.24}$$

The transfer function when the sodium channel is inactive,

$$\frac{V_{out_K}}{V_{in}}(s) = \frac{A_{v_K(s)}}{(s+\tau_K)(s+\tau_{out})}. \tag{4.25}$$

where $A_{v_{Na}}(s)$ and $A_{v_K}(s)$ are the total gain from the sodium and the potassium channels, respectively. $\tau_{D_{Na}}$ and τ_{D_K} are the poles created by each channel's log-domain filters, and $\tau_{D_{out}}$ is the pole created by the membrane capacitor.

By subtracting Eq. (4.24) from Eq. (4.25), we obtain

$$\frac{V_{out}}{V_{in}}(s) = \frac{\left(1-\frac{A_{v_{Na}}(s)}{A_{v_K}(s)}\right)\left(s+\frac{A_{v_K}(s)\cdot\tau_{Na}-A_{v_{Na}}(s)\cdot\tau_K}{A_{v_K}(s)-A_{v_{Na}}(s)}\right)}{(s+\tau_K)(s+\tau_{Na})(s+\tau_{out})}. \tag{4.26}$$

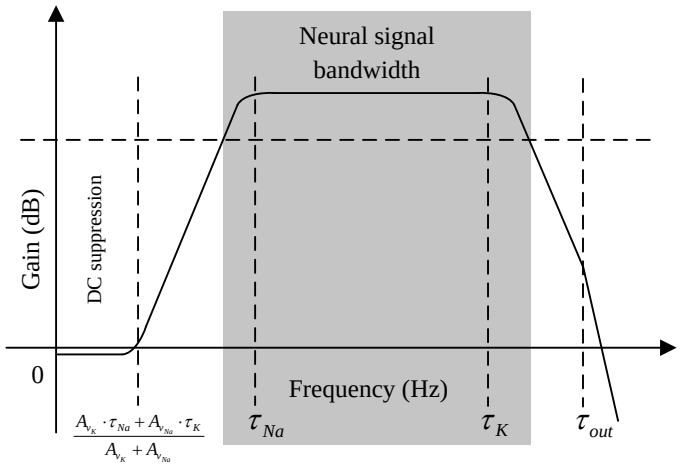

Figure 60: Gain response of the proposed biopotential amplifier. A zero is located at the very beginning. The first and second poles $\tau_{D_{Na}}$ and τ_{D_K} are created by the capacitors in two channels and control the lower and higher cut-off frequencies. The load capacitor contributes the last pole τ_{out}.

The equation (4.26) shows that a zero is created by combining two channels' outputs. By placing the zero ahead of all poles, the system can behave as a bandpass amplifier.

Fig. 60 shows the ideal frequency response - open-loop bandwidth and gain related to the equivalent transfer function as in Fig. 59. The low frequency suppression of the amplifier is due to the negative DC gain up to the *zero* location. The gain starts increasing by 20 dB/dec after the *zero* location. The first pole location gradually diminishes the gain increase resulting in a flat gain level. The second pole eventually lowers the gain beyond the higher cut-off frequency.

The position of the *zero* in the transfer function is controlled by the DC gain and the delay functions from the sodium and the potassium channels. The first pole τ_{Na} is created due to the log-domain filter capacitor of the sodium block. The second pole τ_K is created due to the capacitor in the potassium channel.

Considering the power saving and noise reduction, the sigmoid block has been replaced by a three pair differential linear gain block. The current mirror based log-domain filter has been used to reduce the number of transistors. The circuit schematic of the silicon neuron based biopotential amplifier is shown in Fig. 61.

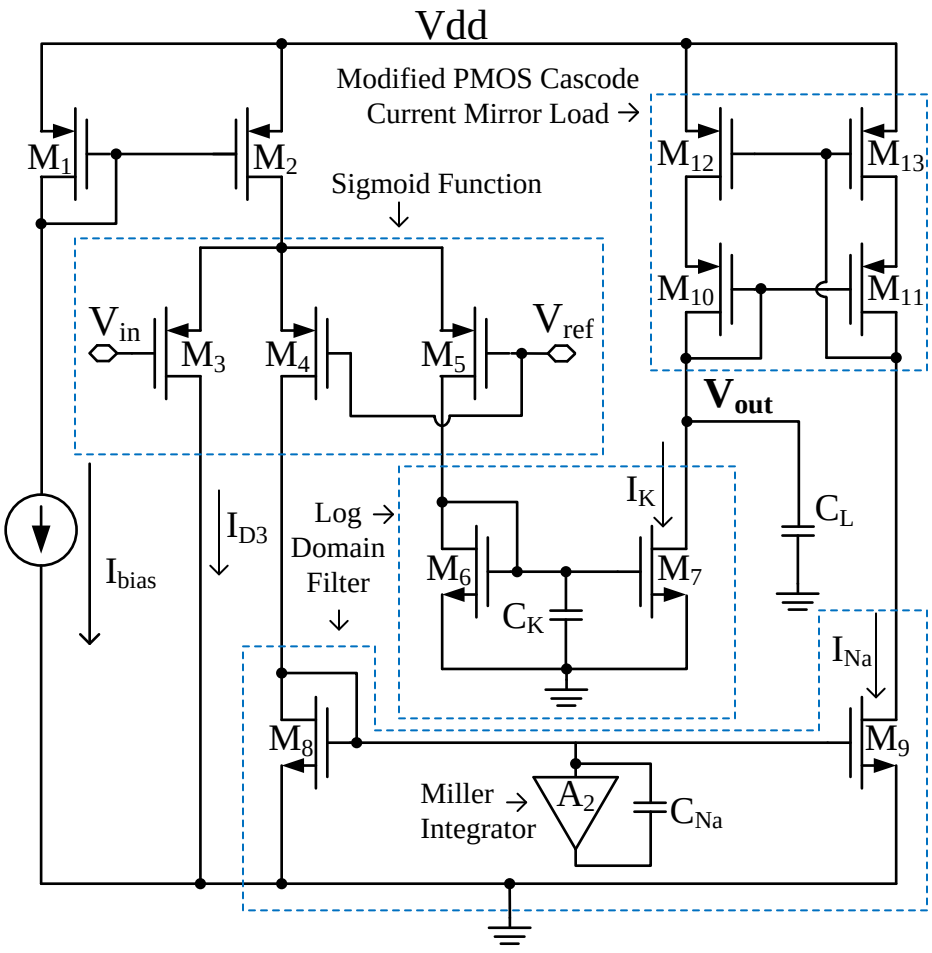

Figure 61: The schematic of the silicon neuron based Biopotential Amplifier and the miller integrator, A2, based capacitor. The sigmoid function is created by a three branch pseudo-differential pair. The log-domain filter is based on the current mirror. The modified PMOS cascode current mirror works as a load and changes the current direction of the sodium current.

The bias current flows into the three branch pseudo-differential pair $M_3 - M_5$ through a PMOS based current mirror. The MOSFETs M_4 and M_5 have the identical dimension and bias voltage, V_{ref}, thus M_4 and M_5 carry the equal drain current. The expressions of the drain currents of M_4 and M_5 are,

$$I_{ref} = I_{D_4} = I_{D_5} = \frac{I_{bias}}{2 + e^{\frac{\kappa\left(V_{in} - V_{ref}\right)}{U_T}}}. \tag{4.27}$$

To simplify the calculation, the linear approximation of the (4.27) is,

$$I_{ref} = I_{D_4} = I_{D_5} = 2 \cdot I_{bias} \frac{\kappa}{U_T} \left(V_{ref} - V_{in}\right), \tag{4.28}$$

where $\kappa \approx 0.7$ is the non-ideality factor, I_{bias} is the bias current from the current source, V_{ref} is the reference voltage, U_T represents the thermal voltage (= $\frac{kT}{q} \approx 25mV$ @27°C), and I_{D_4} and I_{D_5} are the drain currents of M_4 and M_5, respectively.

Different delays τ_{Na} and τ_K are added to the currents from the potassium and the sodium channels by using different values of the capacitors C_{Na} and C_K in the log-domain filters.

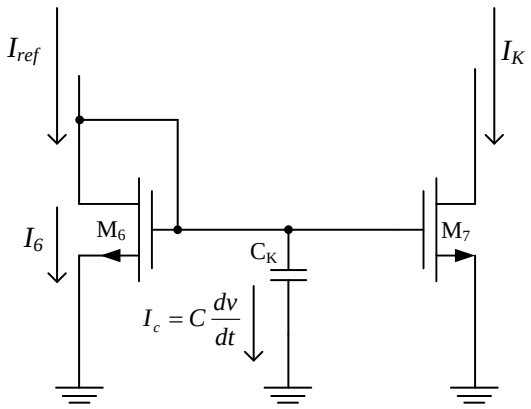

Figure 62: The log-domain filter for the potassium current. I_{ref} is the output current from the sigmoid function, I_K is the output current with delay component, and I_6 is the drain current of M_6.

To improve the noise performance and minimize the number of transistors, the current mirror based log-domain filter has been used. Fig. 62 shows the log-domain block in the potassium channel. A capacitor C_K is connected to the gate terminal of the current mirror that forms a low-pass log-domain structure. The output current I_K from the potassium channel can be expressed as,

$$\frac{dI_K}{dt} = \frac{I_{ref} - I_K}{\frac{C_K U_T}{\kappa I_6}}, \tag{4.29}$$

where I_{ref} is the drain current from M_5 in the differential pair, I_K is the output current with delay component, and I_6 is the drain current from M_6.

The log-domain filter in the sodium channel has exactly the same structure as it is in the potassium channel. However, to decrease the size of the capacitor in the sodium channel, a miller integrator as shown in Fig. 61 has been used. Due to the high gain, low-power, and low-noise requirements of the miller integrator, a cascade class-A amplifier with cascode current mirror load (see Fig. 63) has been used to achieve 40 dB gain with only 1 μW power consumption. By using the miller effect, the capacitor value in the sodium channel has been decreased from 50 nF to 50 pF. Even though the extra amplifier causes 800 nW higher power consumption and 1.2 μV higher input-referred noise, miller capacitor reduces the size of the on-chip capacitor significantly.

The Frequency Response of the Proposed Biopotential Amplifier

Based on Fig. 58, the circuit can be divided into two parts, I_{Na} sourcing current from the sodium channel and I_K sinking current from the potassium channel. The bias current is fed into the two log-domain filter blocks through a three branch pseudo-differential pair as in Fig. 61. Log-domain filters add different delays into I_{Na} and I_K currents. The sodium current I_{Na} charges the load capacitor C_L through a modified cascode current mirror. The potassium current I_K directly discharges the load capacitor C_L.

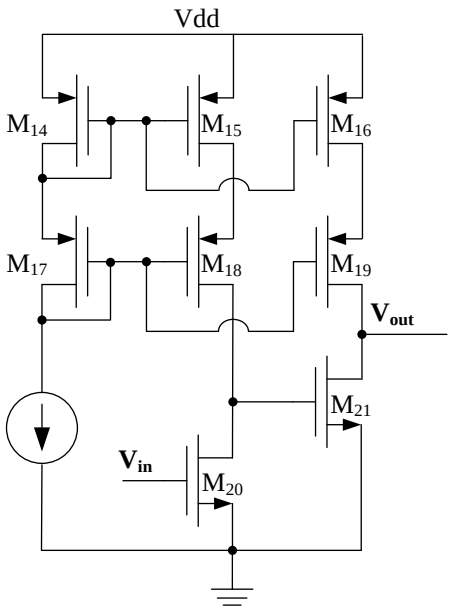

Figure 63: The schematic of the amplifier working as an active miller integrator in the sodium channel log-domain filter. A cascade class-A amplifier with cascode current mirror load can offer 40dB gain.

The frequency response of the output current of the sodium channel is,

$$I_{Na} = \frac{\kappa \cdot I_8 \cdot I_{ref}}{s \cdot A_2 \cdot C_{Na} \cdot U_T + \kappa I_{Na}} \cdot \frac{df}{dfd} \tag{4.30}$$

where I_8 is the drain current of M_8, and A_2 is the gain from the miller integrator.

Similarly, the potassium current I_K can be expressed as,

$$I_K = \frac{\kappa \cdot I_6 \cdot I_{ref}}{s \cdot C_K \cdot U_T + \kappa I_K}. \tag{4.31}$$

where I_6 is the drain current of M_6.

Due to the delay between the two currents, the output current, I_{out}, flows into the load capacitor C_L. The resultant output current can be expressed as,

$$\begin{aligned} I_{out} &= I_{Na} - I_K \\ &= \frac{\kappa I_{ref}((C_K I_8 - A_2 C_{Na} I_6) U_T \cdot s + \kappa(I_8 I_K - I_6 I_{Na}))}{(s \cdot A_2 \cdot C_{Na} \cdot U_T + \kappa I_{Na})(s \cdot C_K \cdot U_T + \kappa I_K)}. \end{aligned} \tag{4.32}$$

The total output impedance including the load capacitor and the current mirror load is,

$$Z_{out} = \frac{1}{C_L\left(s + \frac{1+g_{m_{10}}\left(r_{0_7}+r_{0_{12}}\right)}{C_L \cdot g_{m_{10}} \cdot r_{0_7}\left(1+r_{0_{12}}\right)}\right)}. \tag{4.33}$$

From the Eqs. (4.33) and (4.32), we get the transfer function of the output voltage, V_{out}.

$$\frac{V_{out}}{V_{ref} - V_{in}} = \frac{\alpha \cdot \left(s + \frac{\kappa(I_8 \cdot I_K - I_6 \cdot I_{Na})}{U_T(C_K \cdot I_8 - A_2 \cdot C_{Na} \cdot I_6)}\right)}{\left(s + \frac{\kappa I_{Na}}{A_2 \cdot C_{Na} \cdot U_T}\right)\left(s + \frac{\kappa I_K}{C_K \cdot U_T}\right)\left(s + \frac{1+g_{m_{10}}\left(r_{0_7}+r_{0_{12}}\right)}{C_L \cdot g_{m_{10}} \cdot r_{0_7}\left(1+r_{0_{12}}\right)}\right)} \tag{4.34}$$

where

$$\alpha = \frac{2 \cdot \kappa^2 \cdot I_{bias}\left(C_K \cdot I_8 - A_2 \cdot C_{Na} \cdot I_6\right)}{C_L \cdot U_T^2 \cdot A_2 \cdot C_{Na} \cdot C_K}.$$

The location of the zero is controlled by the bias current, MOSFET transconductance, and log-domain capacitors. The pole locations are mainly dominated by the values of the log-domain capacitors and the load capacitor.

The Pole-Zero Analysis

To achieve the low frequency suppression characteristics, the position of zero must be ahead of the first pole as in Fig. 60. From equation (4.34), the frequency locations of the three poles are,

$$\begin{aligned} \tau_{Na} &= \frac{\kappa I_{Na}}{A_2 \cdot C_{Na} \cdot U_T} \\ \tau_K &= \frac{\kappa I_K}{C_K \cdot U_T} \\ \tau_{out} &= \frac{1 + g_{m_{10}}\left(r_{0_7} + r_{0_{12}}\right)}{C_L \cdot g_{m_{10}} \cdot r_{0_7}\left(1 + r_{0_{12}}\right)}. \end{aligned} \tag{4.35}$$

The *zero* location is defined as,

$$\tau_{zero} = \frac{\kappa(I_8 \cdot I_K - I_6 \cdot I_{Na})}{U_T(C_K \cdot I_8 - A_2 \cdot C_{Na} \cdot I_6)}. \tag{4.36}$$

Because of the miller integrator, the log-domain filter's capacitor in the sodium channel is much bigger than the load capacitor and the capacitor in the potassium channel. As a result, assuming identical magnitudes of the currents I_{Na} and I_K, the value of the τ_{Na} becomes much smaller than the τ_K. The third pole τ_{out} is placed after the τ_K by using a smaller load capacitor value. In this case, the fist pole τ_{Na} is much smaller than the second pole τ_K and the third pole τ_{out}. To justify the frequency location of the *zero* ahead of all the poles, we can compare the values of the τ_{Na}, τ_K, and τ_{out}.

After subtracting the frequency locations of the *zero* and the first pole, we get,

$$\tau_{zero} - \tau_{Na} = \frac{\kappa I_8 \left(A_2 \cdot C_{Na} \cdot I_K - C_K \cdot I_{Na}\right)}{U_T \cdot A_2 \cdot C_{Na} \left(C_K \cdot I_8 - A_2 \cdot C_{Na} \cdot I_6\right)} \tag{4.37}$$

where the numerator is greater than zero for $A_2 \cdot C_{Na} \cdot I_K - C_K \cdot I_{Na} > 0$, and the denominator is smaller than zero for $C_K \cdot I_8 - A_2 \cdot C_{Na} \cdot I_6 < 0$. Equation (4.37) shows that the location of the *zero* is always ahead of the first pole considering the sodium channel's capacitor $A_2 \cdot C_{Na}$ is greater than the potassium channel's capacitor.

The subtraction of the second pole and the third pole is,

$$\tau_K - \tau_{out} = \frac{C_L - C_K \cdot \frac{U_T\left(1+g_{m_{10}}\left(r_{0_7}+r_{0_{12}}\right)\right)}{\kappa I_K \cdot g_{m_{10}} \cdot r_{0_7}\left(1+r_{0_{12}}\right)}}{\frac{C_K \cdot U_T \cdot C_L}{\kappa I_K}}. \tag{4.38}$$

When the load capacitor value is smaller than the capacitor in the potassium channel, the second pole τ_K dominates the higher cut-off frequency.

Noise Analysis

The inversion coefficient (IC) has been used to calculate the input-referred noise and the limit of noise efficiency factor (NEF). The ratio of the division of normalized drain current I_D and the technology specific current I_S is proportional to the level of a MOS transistor's channel inversion [**91**].

$$IC = \frac{I_D}{2n \cdot \mu \cdot U_T \cdot C_{ox} \frac{W}{L}} \tag{4.39}$$

where n is the slop factor, μ is the carrier mobility, and C_{ox} is the gate-oxide capacitance per unite area. IC is between 0.1 to 10 when the transistor is in the weak inversion to moderate inversion. In the strong inversion, IC is greater than 10. From the EKV model the explanation of $\varphi(IC)$ is [**88**]

$$\varphi(IC) = \frac{1}{0.5 + \sqrt{0.25 + IC}}, \tag{4.40}$$

and yields values between 0 and 1.

Due to the large transistor size and low frequency suppression feature from the proposed circuit, the flicker noise is neglected in the noise calculation. The input-referred thermal noise power v_{ni}^2 as a main noise contributor is proportional to the transistor ratio from the differential pair, current mirror, and drain current through the each branch. The noise from the miller integrator is also reflected to the input side. The $v_{ni,total}^2$ for the whole system is ,

$$\begin{aligned} v_{ni,total}^2 =& v_{n3}^2 + 2v_{n4}^2 \left(\frac{g_{m_4}}{g_{m_3}}\right) + 2v_{n8}^2 \left(\frac{g_{m_8}}{g_{m_3}}\right) + 2v_{n7}^2 \left(\frac{g_{m_7}}{g_{m_3}}\right) \\ &+ 2v_{n_{11}}^2 \left(\frac{g_{m_{11}}}{g_{m_3}}\right) + 2v_{n_{12}}^2 \left(\frac{g_{m_{12}}}{g_{m_3}}\right) + 6v_{n_{14}}^2 \left(\frac{g_{m_{14}}}{g_{m_3}}\right) \\ &+ 2v_{n_{20}}^2 \left(\frac{g_{m_{20}}}{g_{m_3}}\right) \end{aligned} \tag{4.41}$$

where v_{ni}^2 equals $4k \cdot n \cdot n \cdot \Gamma_i / g_{m_i} \cdot \Delta f$, and the thermal noise factors Γ_i is $1/2$ for the weak inversion device and $2/3$ for the strong inversion device. Considering that n is a constant, the (4.41) can be written as,

$$
\begin{aligned}
v_{ni,total}^2 = & \frac{4n^2 \cdot U_T \cdot k \cdot T}{I_{D_3} \cdot \varphi(IC_3)} \left(\Gamma_1 + 2\Gamma_4 \frac{\varphi(IC_4)}{\varphi(IC_3)} \beta \right. \\
& + 2\Gamma_8 \frac{\varphi(IC_8)}{\varphi(IC_3)} \beta + 2\Gamma_7 \frac{\varphi(IC_7)}{\varphi(IC_3)} \frac{\beta}{8} \\
& + 2\Gamma_{11} \frac{\varphi(IC_{11})}{\varphi(IC_3)} \frac{\beta}{8} + 2\Gamma_{12} \frac{\varphi(IC_{12})}{\varphi(IC_3)} \frac{\beta}{8} \\
& \left. + 6\Gamma_{14} \frac{\varphi(IC_{14})}{\varphi(IC_3)} \frac{\beta}{\alpha} + 2\Gamma_{20} \frac{\varphi(IC_{20})}{\varphi(IC_3)} \frac{\beta}{\alpha} \right)
\end{aligned}
\tag{4.42}
$$

where

$$
\beta = e^{\frac{\kappa(V_{in} - V_{ref})}{U_T}} \qquad \alpha = \frac{I_{D_3}}{I_{D_{20}}}
$$

To minimize the noise, we use the minimum β value of 1 for equation (4.42), and $\alpha = 0.9$ for the NEF optimization. The transistors in the log-domain filter work in the strong inversion to maintain the low IC. The pseudo-differential pair works in the weak inversion to get the high IC. Operating $M_{6,7,8,9}$ into the weak inversion could push $\varphi(IC_{6,7,8,9})$ downward to 0. Considering all transistors in the weak inversion region having same value of $\varphi(IC_i)$, the minimum input-referred noise can be rewritten as,

$$
v_{ni,total}^2 = \frac{36n^2 \cdot U_T \cdot k \cdot T}{I_{D_3} \cdot \varphi(IC_3)} \cdot \Delta f. \tag{4.43}
$$

Noise Efficiency Factor

To evaluate the noise performance of a low-power biopotential amplifier, a commonly adopted performance metric is the NEF [**92**]. NEF can quantify the noise and the power consumption trade-off in this biopotential amplifier design, and the expression is given by,

$$
NEF = v_{ni,rms} \sqrt{\frac{2 \cdot I_{total}}{4\pi kT \cdot U_T \cdot BW}} \tag{4.44}
$$

where I_{total} is the total current and BW is the bandwidth. By assuming the input transistors operating in the weak-inversion regions, the thermal noise factor $\Gamma_3 = 0.5$, $\varphi(IC_i) = 1$, and $\Delta f = \pi/2 \cdot BW$, the theoretical NEF of the proposed biopotential amplifier with passive capacitor is,

$$NEF = v_{ni,rms}\sqrt{\frac{16n^2}{\varphi(IC_i)}} \approx 5.8. \tag{4.45}$$

The miller integrator will contribute additional current consumption and noise in the active capacitor amplifier structure. We have $I_{total} = I_{total_{main}} + I_{total_{A_2}}$. In this design, the miller integrator results in an increase of the 40% of NEF. The theoretical NEF of the proposed biopotential amplifier with active capacitor is,

$$NEF = v_{ni,rms}\sqrt{\frac{32n^2}{\varphi(IC_i)}} \approx 8.2. \tag{4.46}$$

Results of biopotential amplifier

The proposed biopotential amplifier has been designed in 0.13-μm standard CMOS technology. The bio-inspired neuron structure and sub-threshold MOSFETs have been used to achieve low-power consumption. The charging and discharging profiles of different ionic channels of a Si neuron are utilized to achieve the bandpass low frequency suppression through the combination of two ironic current.

The frequency response of the biopotential amplifier with lower frequency variation is shown in Fig. 64. The proposed biopotential amplifier achieves a gain of 34.51 dB and a -3 dB bandwidth of up to 7 KHz. The lower cut-off frequency can be varied from 11 Hz to 2.5 KHz by the variation of the capacitor in the sodium channel from 50 pF to 2 pF. Fig. 65 shows that the higher cut-off frequency variation from 1.8 KHz to 8.5 KHz with the variation of the capacitor in the potassium channel from 100 pF to 1 pF.

Fig. 66 shows the performance of the proposed biopotential amplifier by using a synthesized spike signal with local field potential. Because of the electrode offset potential

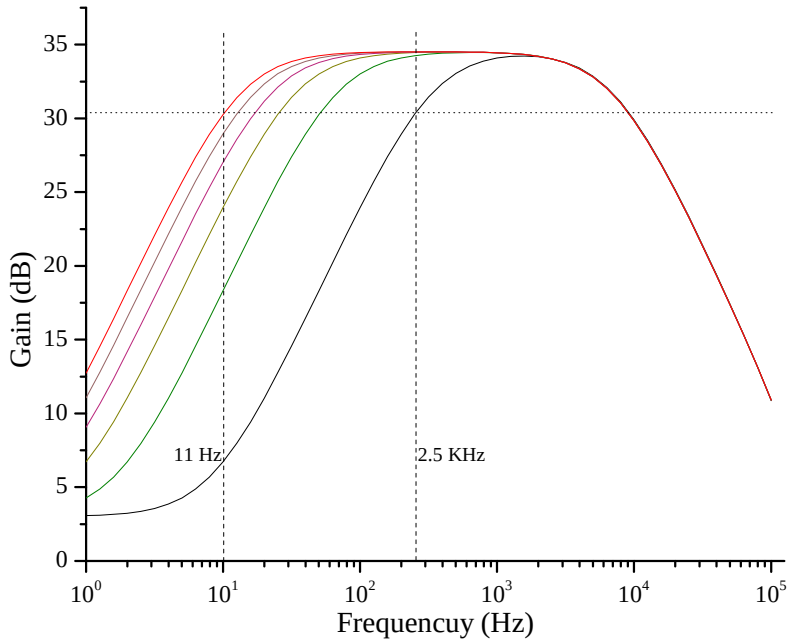

Figure 64: The gain plot of the proposed biopotential amplifier with the variation of lower cut-off frequency from 11 Hz to 2.5 KHz by the variation of the capacitor values in the sodium channel from 50 pF to 2 pF.

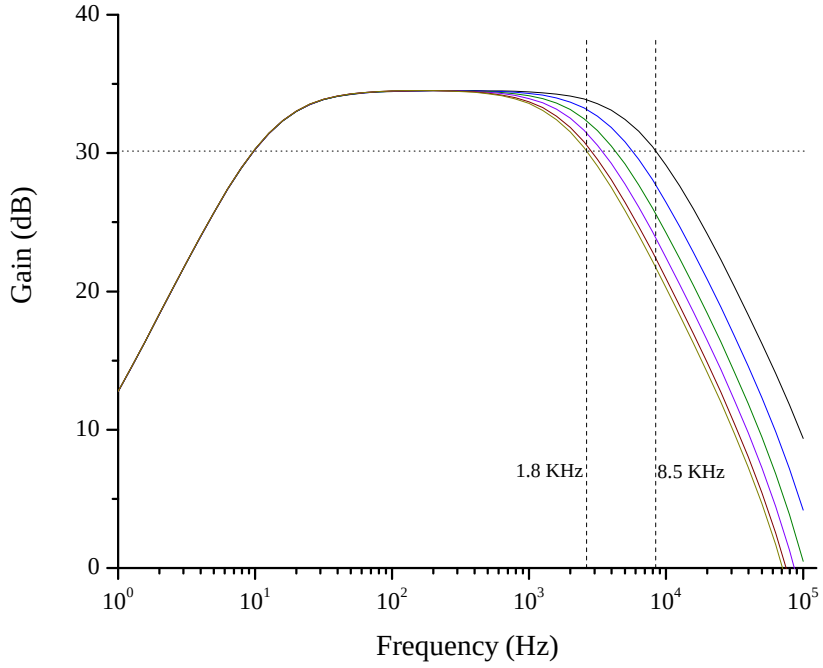

Figure 65: The gain plot of the proposed biopotential amplifier with the variation of higher cut-off frequency from 1.8 KHz to 8.5 KHz by the variation of the capacitor values in the potassium channel from 100 pF to 1 pF.

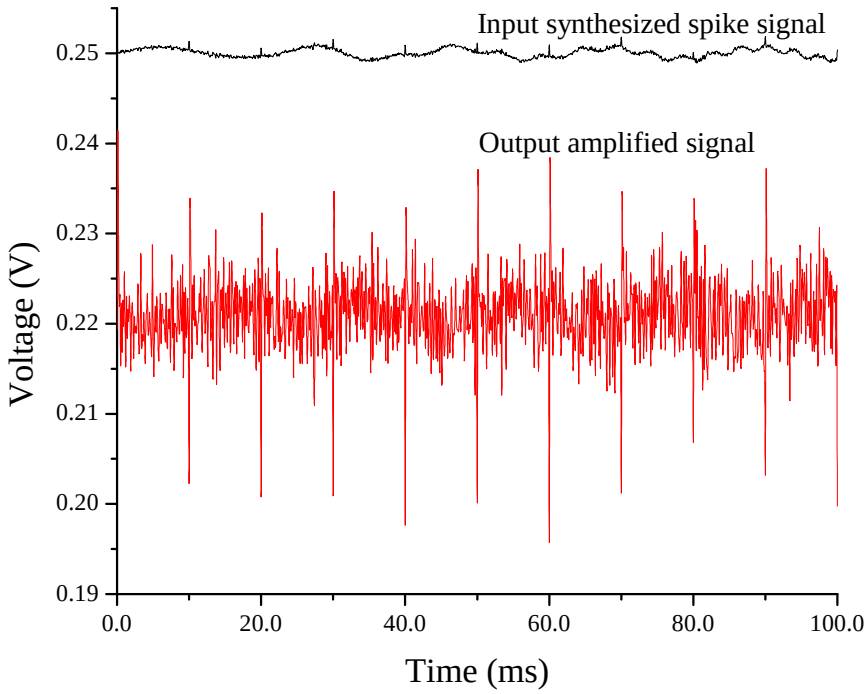

Figure 66: The simulation result of a synthesized spike signal. The input synthesized spike signal with local field potential is on the top. The bottom waveform is the output of the proposed biopotential amplifier.

variation from the tissue, the common interference of the bio-signal can be local field potential (LFPs). LFPs is mainly generated from the neighbouring neurons and movement of electrodes with the amplitude as high as 1 mV with frequency up to 200 Hz[**93**]. The upper waveform in the Fig. 66 is the input synthesized spike signal with noticeable LFPs. The low frequency low frequency suppression of the amplifier suppressed the unwanted LFPs, and only amplified the spike signal showed in the lower section of Fig. 66.

Fig. 67 shows the Monte Carlo simulation results of the integrated input-referred noise due to the device mismatch. An average input-referred noise voltage of 6.6 μV_{rms} is obtained with a standard deviation, $\sigma = 210 \times 10^{-9}$ V. A transient simulation with a sinusoidal input of 200 μV_{p-p} and 1 KHz frequency is performed. The corresponding Monte Carlo simulation as shown in Fig. 43 depicts a total harmonic distortion of 1.3 % with a σ of 0.3.

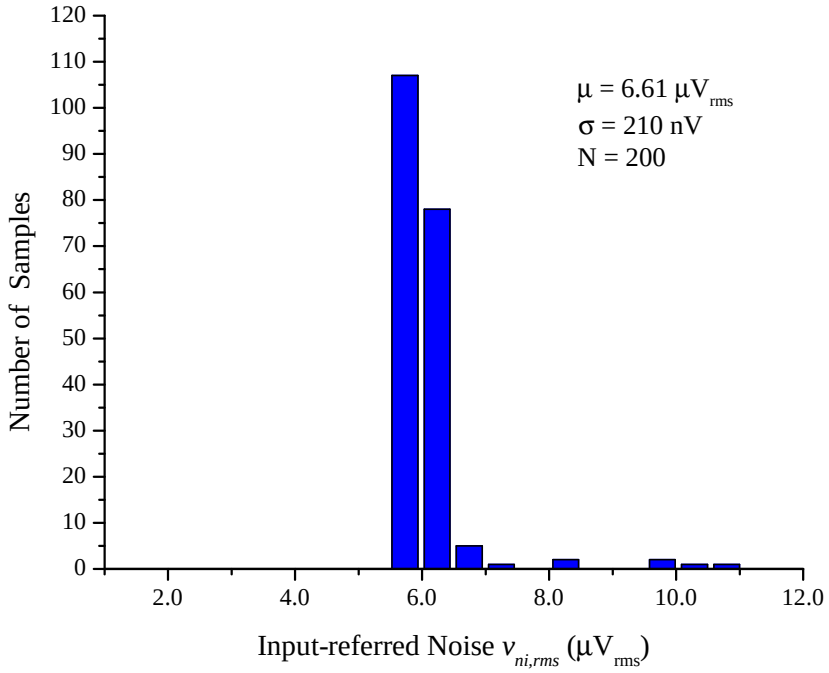

Figure 67: Monte Carlo of the input-referred noise. An average input-referred noise voltage of 6.6 μV_{rms} is obtained with a standard deviation of, $\sigma = 210 \times 10^{-9}$ V.

The passive components has a better noise, power, and NEF, however the capacitor value is 50 nF. From the Table. 6, the miller integrator contributes 1.3 μV extra noise and 1.3 μW power, but it reduces the capacitor value from 50 nF to 50 pF.

Table 6: Performance summary of the proposed biopotential amplifier with the Off-chip Capacitor and the on-chip miller Capacitor

	Off-chip capacitor	miller capacitor
Capacitance	50 nF	50 pF
Gain (dB)	33.7	34.4
Frequency Band	11Hz to 7KHz	11Hz to 7KHz
Input-referred noise (μV_{rms})	5.4	6.6
NEF	6.6	9.2
Max. signal (1% THD) (μV_{p-p})	200	200
Power consumption (μW)	3.6	4.4

Conclusion of the biopotential Amplifier

In this paper, a low-power bio-inspired Hodgkin Huxley silicon neuron based biopotential amplifier has been reported. Two channels of the amplifier, namely a potassium current channel for current sinking and a sodium current channel for current sourcing, are built by pseudo-differential pair and log-domain filters. The sourcing and sinking mechanisms of a silicon neuron are utilized to achieve low frequency suppression and amplification. By placing the poles and zeros at the desired frequency locations, the proposed amplifier achieves the active low frequency suppression. The lower cut-off and higher cut-off frequencies are controlled by the internal capacitors other than the capacitor from the input stage, thus the proposed biopotential amplifier is insensitive to the capacitance variation from the electrode and tissue. The proposed biopotential amplifier can offer a gain of 34 dB with a -3 dB bandwidth of 7 KHz. Although the miller integrator contributes additional noise components and slightly increases the power consumption, it greatly reduces the on-chip capacitor size in the sodium channel from 50nF to 50pF. The lower cut-off frequency and the higher cut-off frequencies can be varied by the variation of the capacitance values in the log-domain filters in the two current channels. The potassium block controls the lower cut-off frequency and the sodium block controls the higher cut-off frequency. The lower cut-off frequency can be varied from 11 Hz to 2.5 KHz, and the higher cut-off frequency can be varied from 1.8 KHz to 8.5 KHz. The amplifier is designed in 0.13 μm standard CMOS process and the total power consumption with 500 mV supply voltage is 4.4 μW. The input-referred noise is 6.7 μV_{rms} integrated over the entire band with a NEF of 9.2. The proposed biopotential amplifier has better power consumption and active electrode-tissue interface variation suppression compare to the recently published works.

Continuous Wavelet Transform

The bio-potential recording system includes low-noise amplifier, filter, analog-to-digital converter (ADC) and signal processing block [**59**]. The amplifier and filter offer the signal

amplification and band selection. The ADC samples and digitizes the signal for further processing. The signal processing block, usually based on software, provides signal analysis tools such as Fourier Transform, Hilbert Transform, and Continuous Wavelet Transform (CWT). The CWT is considered as one of the most useful technique in biosignal processing that offers the localization in both time and frequency for transients, aperiodic and non-stationary signals. The wavelet function facilitates the analysis of the frequency contents of the signal at any particular instance of time. By using different mother wavelet functions and dilation parameters, CWT provides time-frequency analysis on the different types of biosignals. Because of this feature, CWT is widely used in noise reduction [**42**], spike detection [**43**], and seizure detection [**44**].

The conventional CWT is based on software that requires high data rate ADC to minimize the loss of information of the biosignal. The high performance ADC usually has high power consumption [**45**]. However, for applications requiring real-time processing, such as implanted or mobile biomedical devices, low-power consumption is a priority. Hence, the signal processing block should be implemented in hardware instead of software. Even in hardware-based implementation, analog circuits can offer reduced power consumption compared to the digital counter [**47**]. CWT based on an analog filter implementation offers a power-efficient real-time signal processing [**48**].

Wavelet analysis overcomes the inability of Fourier analysis to capture the transients of the time location specific features within a signal. Comparing with the method of Short Time Fourier Transform, wavelets can simultaneously provide the temporal and spectral information of a signal [**95**]. Wavelets have dilation and location parameters, which result in functions that are localized in both time and frequency. The dilation parameter facilitates the wavelet function with a variable window width. In the low-frequency zone, a long time windows are used to get a better low-frequency resolution whereas in the high-frequency zone, a short time windows are used to get finer time information. The CWT can be defined as,

$$T(a,b) = \frac{1}{\sqrt{a}} \int_{-\infty}^{\infty} x(t) \psi^* \left(\frac{t-b}{a} \right) dt \tag{4.47}$$

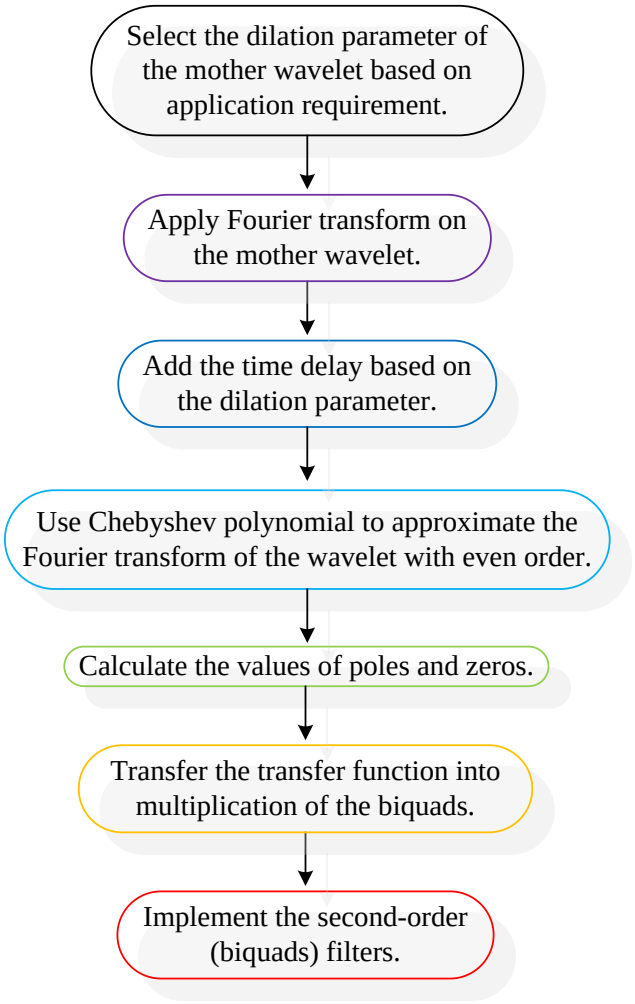

Figure 68: The flow chart of the design procedure of the Continuous Wavelet Transform

where $\psi^*(t)$ is the complex conjugate of the mother wavelet function $\psi(t)$, a is the dilation parameter, and b is the location parameter of the wavelet.

The design steps (in Fig. 68) are: selecting the mother wavelet; taking the Fourier transfer of the desired wavelet; adding delay; applying Chebyshev approximation; calculating the zeros and poles of the transfer function; reconstructing the transfer function; finally implementing the resultant transfer function by using biquads.

Selecting the mother wavelet

The mother wavelet is the function that define the wavelet's function. The mother wavelet, has the feature of orthogonality, compact support, symmetry and vanishing moment. Different mother wavelet will produced different results on the same signals. The Mexican hat, haar, and morlet are considered as one of the most used mother wavelet in the bio-electrical signal [**94**]. In the fellowing processing, the Mexican hat wavelet is chosen for the signal processing unit design.

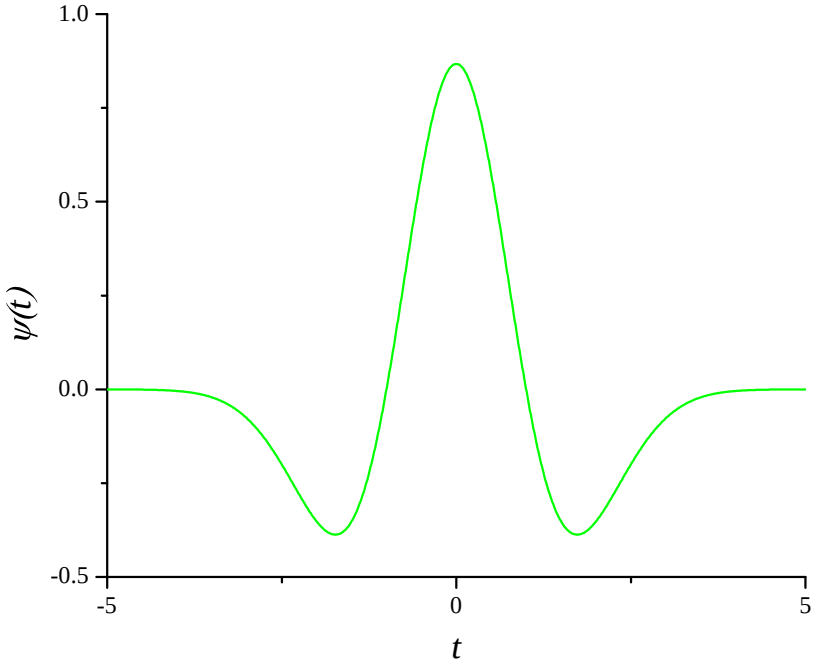

Figure 69: The plot of ideal Mexican hat mother wavelet.

The Mexican hat wavelet is the second derivative of a Gaussian function, and the ideal impulse response is as shown in Fig. 69. The equation of Mexican hat in time domain can be expressed as,

$$\psi_t = \frac{2}{\sqrt{3\sigma}\pi^{\frac{1}{4}}}\left(1-\frac{t^2}{\sigma^2}\right)e^{\frac{-t^2}{2\sigma^2}}. \tag{4.48}$$

where σ is the dilation factor.

Apply Fourier transform on the mother wavelet

The Fourier transform of the Mexican hat mother wavelet function is,

$$\psi(\omega) = \frac{-\sqrt{8}\sigma^{\frac{5}{2}}\pi^{\frac{1}{4}}}{\sqrt{3}}\omega^2 e^{-\frac{\sigma^2\omega^2}{2}}. \tag{4.49}$$

The Fourier transform cannot be directly used in the filter design, so the equation should be transferred into the Laplace domain. The Laplace transform of the Mexican hat mother wavelet is.

$$\psi(s) = \frac{-\pi^{\frac{1}{4}}\sqrt{\frac{8}{3}a^5}s^2}{e^{\frac{-a^2s^2}{2}}} \tag{4.50}$$

It is easy to notice that the original Mexican hat mother wavelet function is y-axis symmetry as in the Fig. 69. However the x-axis, as known as time in the real system, can not be negative. We have to shift the mother wavelet function to the positive axis to avoid the error caused by the negative time axis. In order to get the full conjugate of the signal and wavelet function, a delay must be added in the wavelet.

Adding the time delay

The delayed impulse in the time domain can be found as $\delta(t-\tau)$. The Laplace delay function can be considered as $e^{-\tau s}$, where τ is the length of the delay with unit of second. The Laplace transform of the Mexican hat mother wavelet with delay can be found as

$$H(s) = \frac{-\sqrt{\frac{8}{3}}\pi^{\frac{1}{4}}\sigma^{\frac{5}{2}}s^2}{e^{\tau s-\frac{-\sigma^2s^2}{2}}}. \tag{4.51}$$

Since (4.51) has exponential term in the denominator, the transfer function can not be realized into a standard form. Hence, the exponential term needs to be expanded.

The easiest and most common way to approximate the expectational function is using Taylor expansion. However the Taylor expansion with Maclaurin's series is accurate only when σ is near zero, but becomes increasingly inaccurate with σ increases. The Chebyshev polynomial with a better accuracy approximation can significantly decrease the polynomial . Decreasing the degree number can significantly decrease the circuit design complexity and the power consumption. In order to use fewer terms approximation with high accuracy, we have selected the Chebyshev polynomials.

Chebyshev polynomials are a sequence of orthogonal polynomials that can be written as monic polynomials of n^{th} degree whose deviation from zero is as small as possible. Using a series based on orthogonal Chebyshev polynomials on approximating large systems of equations gives better results in terms of accuracy than the typical methods such as the mean square approximation or the Taylor approximation [**96**].

The recurrence relation of Chebyshev polynomials with arbitrary interval a can be found as,

$$\left.\begin{aligned} T_0(x) &= 1 \\ T_1(x) &= \frac{x}{a} \\ T_2(x) &= \frac{2x}{a}T_1(x) - T_0(x) \\ &\vdots \\ T_n(x) &= \frac{2x}{a}T_{n-1}(x) - T_{n-2}(x) \end{aligned}\right\} \quad for\, x \in [-a, a]\,. \tag{4.52}$$

The coefficients of the Chebyshev polynomials corresponding to the each order of the s can be found as,

$$c_{o_n} = \frac{1}{C_n(s)} \int_{-a}^{a} W(s) \cdot T_n(s) \cdot f(s)\, ds. \tag{4.53}$$

where a is the approximation interval related to the accuracy of the approximation, $f(x)$ is the function needed be approximated, $T_n(s)$ is the Chebyshev polynomial corresponding

with turns, $W(s)$ is the scale function related to a, and $C_k(x)$ is the weight function which can be found below. The weight function $C_k(s)$ in the interval of $[-a,a]$ is,

$$C_k(s) = \int_{-a}^{a} W(s) \cdot T_n^2(s)\, ds$$

$$\textit{where} \tag{4.54}$$

$$W(s) = \frac{1}{\sqrt{a^2 - s^2}}.$$

We have use the MATLAB code to do the Chebyshev approximation. The codes are

```
clear all
clc
a = input('Interval of x [-a,a] a=');
n = input('Number of turns n=');
syms x;
c = 0.2;
tao = 0.8;
M_hat_1 = exp(x*tao-c^2*x^2/2);
Haar = x*exp(x/2+tao*x);
f = M_hat_1;
W = 1/sqrt(a^2-x^2);
T = [1 x/a];
Tayl = taylor(f,n);
for i=3:n
    T(i)= expand(2*(x/a)*T(i-1) - T(i-2));
end
Chyb = 0*x;
for j=1:n
C = int(W*(T(j))^2,-a,a);
```

```
r = vpa(1/C*int(W*f*T(j),-a,a),10);
Chyb = Chyb + r*T(j)
end
Tayl = taylor(f,n);
```

With a dilation factor $\sigma = 0.2$ and delay $\tau = 0.8$, the center frequency of the wavelet is found to be 1 Hz. The interval $a = 3$ is selected based on the center frequency of the mother wavelet. The first terms of coefficients of the Chebyshev polynomial corresponding with the function $e^{0.8s-0.02s^2}$ can be calculated as,

$$c_{o_0} = \frac{1}{\int_{-3}^{3} \frac{1}{\sqrt{3^2-s^2}} \cdot 1^2 \, ds} \int_{-3}^{3} \frac{1}{\sqrt{3^2-s^2}} \cdot 1 \cdot e^{0.8s-0.02s^2} \, ds. \tag{4.55}$$

The rest coefficients can be calculated by the method provided in (4.53). Finally the approximated transfer function is shown,

$$\begin{aligned} H(s) = \frac{-0.0389s^2}{0.011999853794280714727977842784763s^4} \\ +0.082948231213368508144515537331379s^3 \\ +0.296199087631179461112108776256 31s^2 \\ +0.769154217916028601932191636573 56s \\ +1.001894393842919726497764365547 \end{aligned} \tag{4.56}$$

The Chebyshave approximation has a higher accuracy approximation than Taylor. To compare the performance, we have use Taylor to expand the (4.55). Fig. 70 is the performance comparison of the Chebyshev approximation and Taylor approximation on the Mexican hat wavelet. The plots show percentage error of the 4^{th} order Chebyshev and the 4^{th} order Taylor approximations of the denominator with $\sigma = 0.2$ and $\tau = 0.8$ in the interval of -3 to 3. The maximal error of Taylor approximation reaches 40%. However, the maximal error of Chebyshev approximation is only 6%.

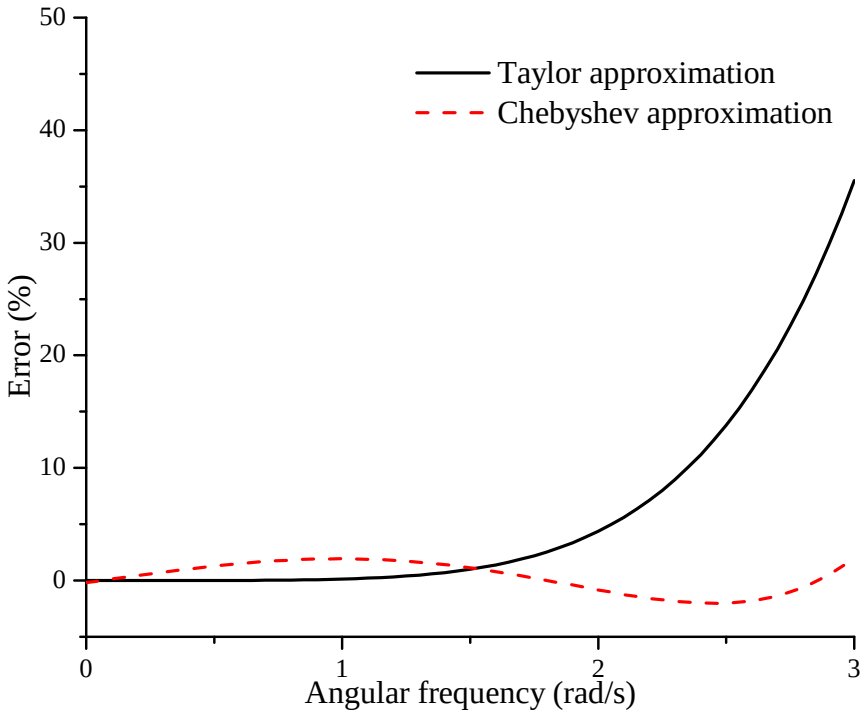

Figure 70: The maximal error of Taylor approximation reaches to 40%, however the maximal error of Chebyshev approximation is only 6%.

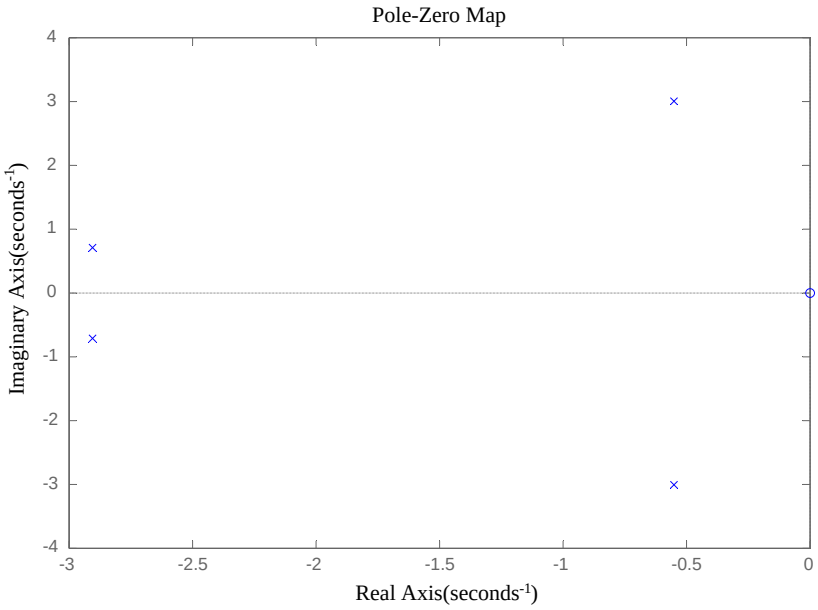

Figure 71: The poles and zeros plot corresponding with equation (4.56)

Poles and zeros calculation

The values of four poles and two zeros can be calculated from (4.56). The zeros and poles position can be also found in the Fig. 71. They are $s_1 = -2.91 - j0.71$, $s_2 = -2.91 + j0.71$, $s_3 = -0.551 - j3.011$, $s_4 = -0.551 + j3.011$, and $z_1 = z_2 = 0$.

After the value of poles and zeros are calculated form (4.56), a new biquads transfer function can be written as,

$$H(s) = \frac{s^2}{s^2 + 36.568138s + 354.208258} \cdot \frac{-0.0389}{s^2 + 6.92407s + 369.90179795}. \tag{4.57}$$

The new transfer function (4.57) indicates that the Mexican hat wavelet can be easily implemented by cascading a second-order high-pass filter and a second-order low-pass filter.

Biquads transfer function construction

The transfer function (4.57) can be implemented by LC ladder, Gm-C, or log-domain structures. The functional block implementations of the transfer function (4.57) is shown in Fig. 72. The first stage is a second-order high-pass filter with two zeros at the origin. The second stage is a second-order low-pass filter that generates the third and fourth poles for the system. The last stage, a gain-control stage, can normalize the output signal. The first and the second stage can be performed either by passive structures, such as LC ladder and RC filter or active structures, such as single-amplifier biquad filter, butter-worth biquad, and Sallen-Key circuits *et al*; or other MOSFET based structures, such as Gm-C filter and log-domain filter.

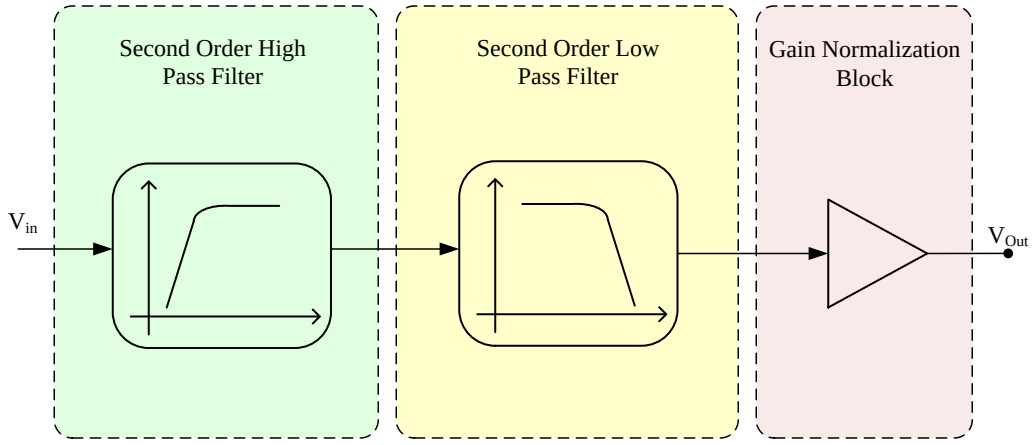

Figure 72: Functional block level implementations of the transfer function as shown in (4.57).

Analog CWT filter simulation

In order to verify An OTA based 4^{th} order Mexican hat wavelet filter has been designed and simulated by Cadence. The circuit diagram of the analog CWT filter is shown in Fig. 73. The first block is a high pass filter with the transfer function of $\frac{s^2}{s^2+36.568138s+354.208258}$. The second block is a low pass filter with the transfer function of $\frac{1}{s^2+6.92407s+369.90179795}$. And the third block is an inverting amplifier that turns the output gain and sign. The components

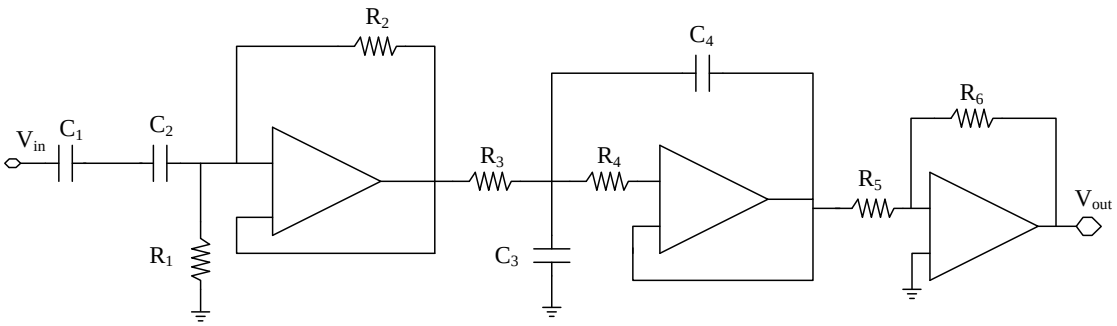

Figure 73: The circuit implementation of the analog CWT filter

value can be found in the Table 7

Table 7: The components vale of analog CWT filter

Component Name	Components' value
C_1	10.8 pF
C_2	10 pF
C_3	1 pF
C_4	22 pF
R_1	6.4695 GΩ
R_2	5.41 GΩ
R_3	11 GΩ
R_4	9.7 GΩ
R_5	1 GΩ
R_6	350 MΩ

The impulse response of the proposed filter is shown in Fig. 74 The black plot is the input impulse that is generated by pulse generator with an amplitude of 1 V, pulse width of 100 ms and delay of 500 ms. The red plot is the output of the Mexican hat wavelet corresponding to the impulse signal.

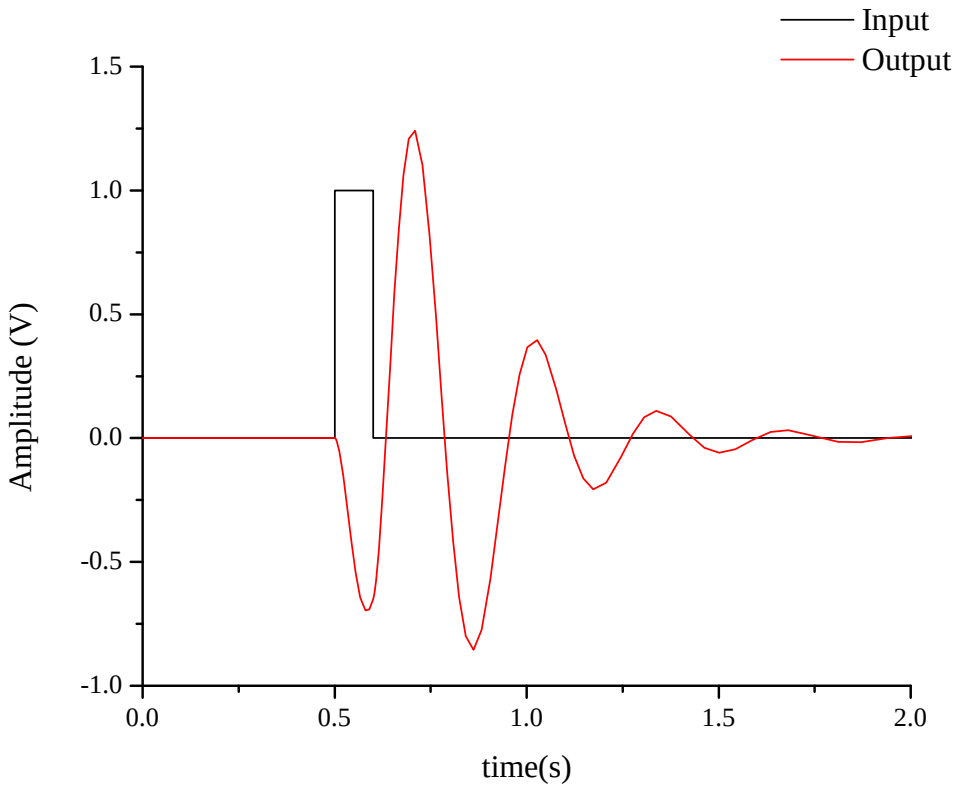

Figure 74: The impulse response of the analog CWT filter.

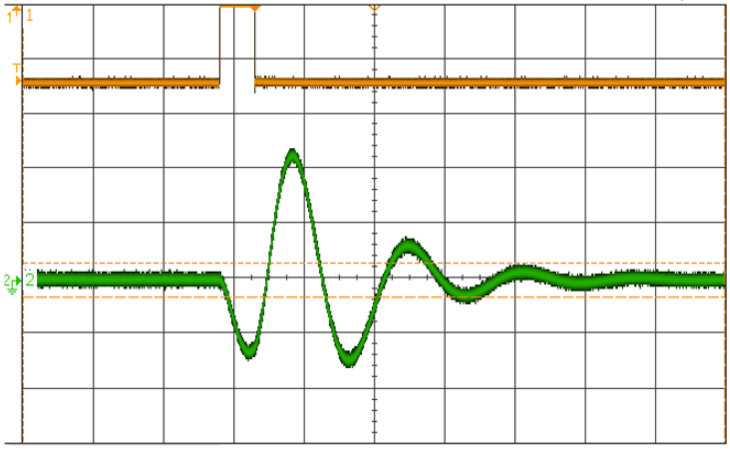

Figure 75: The upper plot is the input impulse with amplitude of 1 V, 100 ms pulse width and 500 ms delay. The lower plot is the impulse response output of the Mexican hat wavelet.

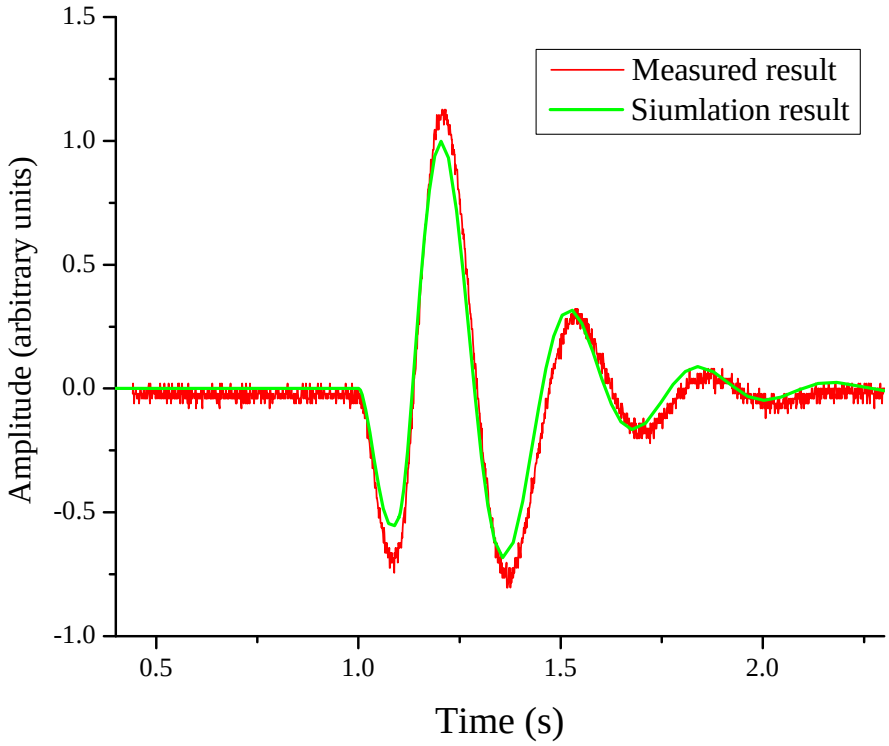

Figure 76: The comparison of measured result of the impulse response versus the simulation results.

In order to proof-of-concept of the proposed method, a board level design is an implementation by using AD8044. The proposed method can be easily implemented by using three OPAMPs based units - a high pass filter, a low pass filter, and an inverting amplifier.

Fig. 75 is the impulse response of the Mexican hat wavelet measured by oscillator scope. The upper plot is the input impulse that is generated by function generator with an amplitude of 1 V, pulse width of 100 ms and delay of 500 ms. The lower plot is the output of the Mexican hat wavelet corresponding to the impulse signal.

Fig. 76 shows the comparison of the measured result and the simulation result. Although the passive components have value variation and the mismatch, the measurement results show a high similarity to the simulation result.

Switched capacitor CWT filter

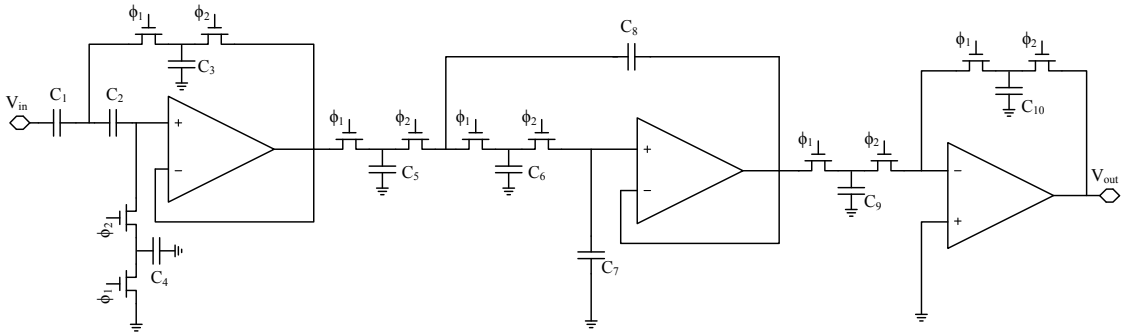

Figure 77: The schematic of the switched capacitor CWT filter.

The proposed circuit is also designed and simulated by using a switched capacitor structure. As we can see from the Table7, the resistors' value are very high. The GΩ resistor requires a significant amount of chip area. In additional, the resistor's variation can reach 15%. In order to minimize the value and variation of resistors, the switched capacitor technology is used in this design. The schematic of switched capacitor CWT filter is shown in Fig. 77. All resistors are replaced by two switch MOSFETs and capacitor. The size of

the MOSFET is 500nm wide and 500nm length. The switching frequency is 100Hz. The capacitors value can be found in the Table 8.

Table 8: The capacitors vale of switched capacitor CWT filter

Component Name	Components' value
C_1	10.8 pF
C_2	10 pF
C_3	1.84 pF
C_4	1.54 pF
C_5	0.909 pF
C_6	1.03 pF
C_7	1 pF
C_8	22 pF
C_9	1 pF
C_{10}	2.5 pF

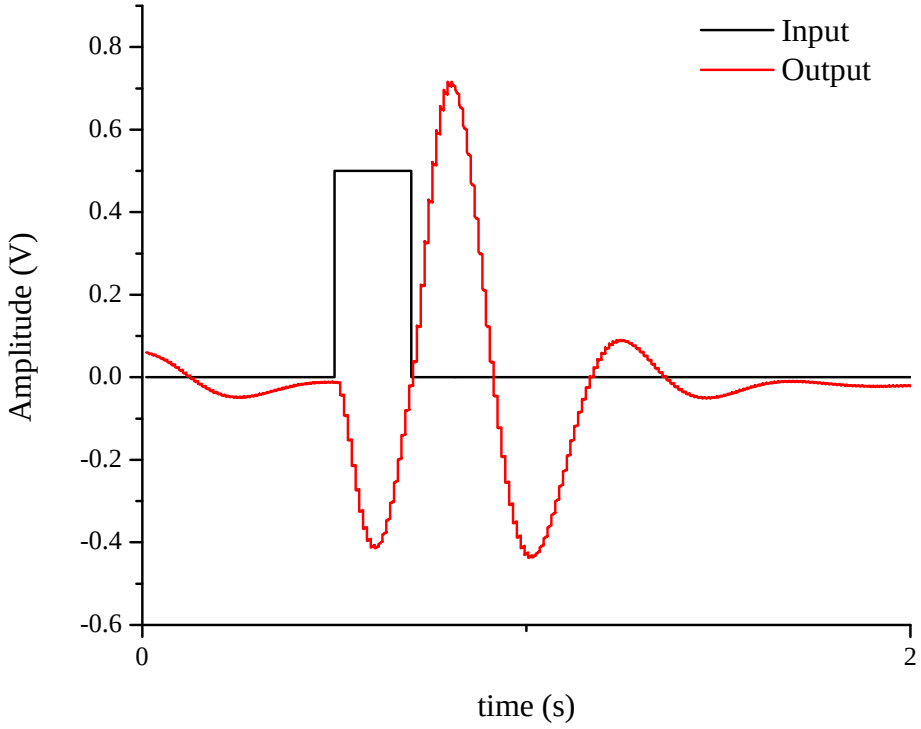

Figure 78: The implementation of the switched capacitor wavelet transform.

In the Fig. 78, the block line is input pulse signal with the pulse width of 100 ms with delay of 500 ms and amplitude of 1V. The red line is the output signal. The output signal

of switched capacitor filter shows less extra oscillation compared to the pure analog CWT filter in Fig. 74.

Conclusion of wavelet

The 4^{th} order Chebyshev approximation has been applied in the Mexican hat wavelet function to achieve a high accuracy with relatively lower degree approximation. The transfer function of the wavelet is reconfigured into the multiplication of two biquad filters to simplify the circuit implementation further. For the proof-of-concept, a circuit implementation of the Mexican hat wavelet function is tested on the board level. The results show that the proposed design process offers a higher accuracy approximation and less complicated method in analog wavelet transform circuit implementation.

We developed a unique method to simplify the analog wavelet filter design. The 4^{th} order Chebyshev approximation is applied in the Mexican hat wavelet function to achieve greater accuracy with relatively lower degree transfer function. The transfer function of the wavelet is reconstructed into the multiplication of two biquad filters to simplify the circuit implementation further. For the proof-of-concept, a circuit implementation of Mexican hat wavelet-based on the proposed method is tested. The results show that the proposed design process offers a higher accuracy approximation and less complicated method in analog wavelet transform circuit implementation.

This paper presented a method on the implementation of a continuous time wavelet transformation by using the biquads, with the motivation of simplifying the circuit implementation. The Chebyshev approximation of Mexican hat wavelet shows better accuracy compared to Taylor expansion in 4^{th} order. The maximal error of Taylor approximation reaches 40% whereas the maximal error of Chebyshev approximation is only 6%. A new transfer function was reconstructed into the form of multiplication of biquads. By cascading biquads, the complexity of higher-order filter circuit implementation of is significantly reduced. As a proof-of-concept, a circuit implementation of Mexican hat wavelet has been implemented. The experimental result and the simulation result show a close match. The

proposed the method offers estimate with greater accuracy and easier way to implement the analog continuous wavelet transform circuit.

CONCLUSIONS AND FUTURE RESEARCH

The implantable device is booming very faster science the first cochlear implant introduced 50 years ago. Brain and neural implants are becoming one of the hottest topics both in the industry and academic. Because the implantable devices have the feature of small size and low power consumption, the brain implants have a great potential in medical device market.

A typical implanted signal recording system has four major blocks, a powering unit, a signal processing unit, a data conversion unit, and a wireless communication unit. For the propose of powering saving, this dissertation proposed new methods both in the powering unit and signal processing unit.

In the powering unit, a power sending circuit and a recovering circuit are presented. The power-oscillator closely follows the frequency of the injection signal and sustains the performance irrespective of the supply voltage variation. The differential cross-coupled power-oscillator showed more than 90% constant link efficiency in the 20% of a supply voltage variation. A modified class-E type CMOS differential cross-coupled rectifier circuit is designed. Simulation results indicate a PCE of 92% for an input signal of 7 MHz, 2 V (peak) with a load resistance of 100 Ω.

In the signal processing unit, an amplifier filter bank and a bio-inspire amplifier are designed. In order to decrease the data volume, a new method of CWT is given. The bio-inspired circuit design method is used in the bio-amplifier and amplifier filter design for the proposed of power saving. The implementation of the silicon neural is presented to explain the method of the low power design. The current sourcing and the current sinking mechanisms are used in the amplifier-filter and bio-inspired amplifier design to decrease the total power consumption. The proposed amplifier-filter bank is designed in 0.13-μm

standard CMOS process, and the resultant structure consumes a total of 1.8525 μW with 1 V supply voltage. The system contains four amplifier-filter bank with the signal band coverage of 40 Hz to 10.8 KHz and shows NEF of approximately 3 per channel. The proposed biopotential amplifier has better power consumption and active electrode-tissue interface variation suppression compare to the recently published works. The lower cut-off frequency can be varied from 11 Hz to 2.5 KHz, and the higher cut-off frequency can be varied from 1.8 KHz to 8.5 KHz. The total power consumption with 500 mV supply voltage is 4.4 μW. The input-referred noise is 6.7 μV_{rms} integrated over the entire band with an NEF of 9.2.

In the CWT design, a new method is produced for the purpose of circuit complexity reduction. The 4^{th} order Chebyshev approximation is applied in the expansion of the Mexican hat mother wavelet. The Chebyshev approximation achieves a high accuracy with the less degree of a polynomial. The transfer function of the wavelet is reconstructed into the multiplication of two biquad filters based on the poles and zeros location. A CWT filter in analog structure and mixed signal by using cadence is designed and tested. The OPAMP based PCB level implementation is also presented in the dissertation.

This dissertation presented a design of the analog signal processing unit for implantable wirelessly-powering recording system. Although some pre-research on the powering unit is presented, the coil design is not discussed in this dissertation. The coil design, the data conversion unit and the wireless communication unit are great topics for further research.

REFERENCE

[1] Q. Ma, M. Haider, V. Shrestha, and Y. Massoud, "Bursting hodgkin huxley model based ultra low power neuromimetic silicon neuron," *Analog Integrated Circuits and Signal Processing*, pp. 1–9, 2012, 10.1007/s10470-012-9888-6.

[2] L. R. Hochberg, M. D. Serruya, G. M. Friehs, J. A. Mukand, M. Saleh, A. H. Caplan, A. Branner, D. Chen, R. D. Penn, and J. P. Donoghue, "Neuronal ensemble control of prosthetic devices by a human with tetraplegia," *Nature*, vol. 442, pp. 164–171, 2006.

[3] O. Majdalawieh, J. Gu, T. Bai, and G. Cheng, "Biomedical signal processing and rehabilitation engineering: a review," in *Communications, Computers and signal Processing, 2003. PACRIM. 2003 IEEE Pacific Rim Conference on*, vol. 2, 2003, pp. 1004–1007 vol.2.

[4] N. Thakor and Y.-S. Zhu, "Applications of adaptive filtering to ecg analysis: noise cancellation and arrhythmia detection," *Biomedical Engineering, IEEE Transactions on*, vol. 38, no. 8, pp. 785–794, 1991.

[5] H. Gholam-Hosseini, H. Nazeran, and K. Reynolds, "Ecg noise cancellation using digital filters," in *Bioelectromagnetism, 1998. Proceedings of the 2nd International Conference on*, 1998, pp. 151–152.

[6] S. Charleston and M. Azimi-Sadjadi, "Reduced order kalman filtering for the enhancement of respiratory sounds," *Biomedical Engineering, IEEE Transactions on*, vol. 43, no. 4, pp. 421–424, 1996.

[7] E. A. Clancy, E. L. Morin, and R. Merletti, "Sampling, noise-reduction and amplitude estimation issues in surface electromyography," *Journal of Electromyography and Kinesiology*, vol. 12, no. 4, p. 116, February 2002.

[8] G. Bonmassar, P. L. Purdon, I. P. Jaaskelainen, K. Chiappa, V. Solo, E. N. Brown, and J. W. Belliveau, "Motion and ballistocardiogram artifact removal for interleaved recording of eeg and eps during mri," *Neuroimage*, vol. 16, no. 4, p. 11271141, August 2002.

[9] S. P. Strong, R. Koberle, R. R. de Ruyter van Steveninck, and W. Bialek, "Entropy and information in neural spike trains," *Phy. Rev. Let.*, vol. 80, no. 4, pp. 197–200, 1998.

[10] Greatbatch, Wilson, and C. Holmes, "History of implantable devices," *Engineering in Medicine and Biology Magazine, IEEE*, vol. 10, no. 3, pp. 38–41, Sept 1991.

[11] C. W, G. A, and G. W, "A transistorized, self-contained, implantable pacemaker for the long-term correction of complete heart block." *Surgen*, vol. 48, 1960.

[12] B. Barouh, "Heart-beat pacing apparatus," Oct. 10 1967, uS Patent 3,345,990. [Online]. Available: http://www.google.com/patents/US3345990

[13] G. Antonioli, F. Baggioni, F. Consiglio, G. Grassi, R. LeaBrun, and F. Zanardi, "Stinulatore cardiaco impiantabile con nuova battaria a stato solido al litio," *Minerva Med*, vol. 64, p. 2298, 1973.

[14] P. J. Blackshear, F. D. Dorman, P. L. Blackshear, R. L. Varco, and H. Buchwald, "A permanently implantable self-recycling low flow constant rate multipurpose infusion pump of simple design." *Surgical forum*, vol. 21, 02/1970.

[15] F. W. Casadei, M. Gerold, and E. Baldinger, "Implantable blood pressure telemetry system," *Biomedical Engineering, IEEE Transactions on*, vol. BME-19, no. 5, pp. 334–341, Sept 1972.

[16] M. M, "The implantable cardioverter-defibrillator: an update," . *J Cardiovascular Med*, vol. 9, p. 191, 1984.

[17] C. D. Saudek, J.-L. Selam, H. A. Pitt, K. Waxman, M. Rubio, N. Jeandidier, D. Turner, R. E. Fischell, and M. A. Charles, "A preliminary trial of the programmable implantable medication system for insulin delivery," *New England Journal of Medicine*, vol. 321, no. 9, pp. 574–579, 1989, pMID: 2761602. [Online]. Available: http://www.nejm.org/doi/full/10.1056/NEJM198908313210904

[18] . T. R, T. WB, and Z. J, "An implantable neurocybemetic prosthesis system," *Epilepsia*, vol. 1, p. 33, 1990.

[19] D. Jeutter and F. Josse, "Design of a radio-linked implantable cochlear prosthesis using surface acoustic wave devices," *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on*, vol. 40, no. 5, pp. 469–477, Sept 1993.

[20] H. Matsuki, K. Ofuji, N. Chubachi, and S. Nitta, "Signal transmission for implantable medical devices using figure-of-eight coils," *Magnetics, IEEE Transactions on*, vol. 32, no. 5, pp. 5121–5123, Sep 1996.

[21] T. Akin, K. Najafi, and R. Bradley, "A wireless implantable multichannel digital neural recording system for a micromachined sieve electrode," *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 1, pp. 109–118, Jan 1998.

[22] T. Berger, M. Baudry, R. Brinton, J.-S. Liaw, V. Marmarelis, A. Yoondong Park, B. Sheu, and A. Tanguay, "Brain-implantable biomimetic electronics as the next era in neural prosthetics," *Proceedings of the IEEE*, vol. 89, no. 7, pp. 993–1012, Jul 2001.

[23] J. Yao and Y.-T. Zhang, "The application of bionic wavelet transform to speech signal processing in cochlear implants using neural network simulations," *Biomedical Engineering, IEEE Transactions on*, vol. 49, no. 11, pp. 1299–1309, Nov 2002.

[24] M. Min, T. Parve, V. Kukk, and A. Kuhlberg, "An implantable analyzer of bio-impedance dynamics: mixed signal approach [telemetric monitors]," *Instrumentation and Measurement, IEEE Transactions on*, vol. 51, no. 4, pp. 674–678, Aug 2002.

[25] S. A. P. Haddad, R. Houben, and W. Serdijn, "Analog wavelet transform employing dynamic translinear circuits for cardiac signal characterization," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 1, May 2003, pp. I–121–I–124 vol.1.

[26] M. Astrom, S. Olmos, and L. Sornmo, "Wavelet-based event detection in implantable cardiac rhythm management devices," *Biomedical Engineering, IEEE Transactions on*, vol. 53, no. 3, pp. 478–484, March 2006.

[27] A. Kamboh, M. Raetz, K. Oweiss, and A. Mason, "Area-power efficient vlsi implementation of multi-channel dwt for data compression in implantable neuroprosthetics," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 1, no. 2, pp. 128–135, June 2007.

[28] K. G. Oweiss, A. Mason, Y. Suhail, A. Kamboh, and K. Thomson, "A scalable wavelet transform vlsi architecture for real-time signal processing in high-density intra-cortical implants," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 54, no. 6, pp. 1266–1278, June 2007.

[29] V. Gopalakrishna, N. Kehtarnavaz, and P. Loizou, "A recursive wavelet-based strategy for real-time cochlear implant speech processing on pda platforms," *Biomedical Engineering, IEEE Transactions on*, vol. 57, no. 8, pp. 2053–2063, Aug 2010.

[30] A. Casson and E. Rodriguez-Villegas, "A 60 pw gm c continuous wavelet transform circuit for portable eeg systems," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 6, pp. 1406–1415, June 2011.

[31] R. Olsson and K. Wise, "A three-dimensional neural recording microsystem with implantable data compression circuitry," in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, 2005, pp. 558–559 Vol. 1.

[32] R. Harrison, P. Watkins, R. Kier, R. Lovejoy, D. Black, B. Greger, and F. Solzbacher, "A low-power integrated circuit for a wireless 100-electrode neural recording system," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 1, pp. 123–133, 2007.

[33] A. Sodagar, G. Perlin, Y. Yao, K. Najafi, and K. Wise, "An implantable 64-channel wireless microsystem for single-unit neural recording," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 9, pp. 2591–2604, 2009.

[34] R. Harrison and C. Charles, "A low-power low-noise cmos amplifier for neural recording applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958 – 965, june 2003.

[35] F. Zhang, J. Holleman, and B. Otis, "Design of ultra-low power biopotential amplifiers for biosignal acquisition applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, no. 4, pp. 344 –355, aug. 2012.

[36] V. Majidzadeh, A. Schmid, and Y. Leblebici, "Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 5, no. 3, pp. 262–271, 2011.

[37] K. Abdelhalim and R. Genov, "Compact chopper-stabilized neural amplifier with low-distortion high-pass filter in 0.13um cmos," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, may 2012, pp. 1075 –1078.

[38] K. Odame and P. Hasler, "An adaptive quality-factor bandpass filter," in *2007 IEEE International Symposium on Circuits and Systems (ISCAS)*, may 2007, pp. 3295 –3298.

[39] P. Corbishley and E. Rodriguez-Villegas, "A nanopower bandpass filter for detection of an acoustic signal in a wearable breathing detector," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, no. 3, pp. 163 –171, sept. 2007.

[40] S.-C. Lee, S.-Y. Lee, and C.-H. Chiang, "0.9 v low-power switched-opamp switched-capacitor bandpass filter for electroneurography acquisition systems," *Circuits, Devices Systems, IET*, vol. 2, no. 2, pp. 257 –263, april 2008.

[41] B. Rumberg and D. Graham, "A low-power and high-precision programmable analog filter bank," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 59, no. 4, pp. 234–238, 2012.

[42] J. Lewis and C. Burrus, "Approximate continuous wavelet transform with an application to noise reduction," in *Acoustics, Speech and Signal Processing, 1998. Proceedings of the 1998 IEEE International Conference on*, vol. 3, 1998, pp. 1533–1536 vol.3.

[43] M. Faezipour, T. Tiwari, A. Saeed, M. Nourani, and L. Tamil, "Wavelet-based denoising and beat detection of ecg signal," in *Life Science Systems and Applications Workshop, 2009. LiSSA 2009. IEEE/NIH*, 2009, pp. 100–103.

[44] H. Vavadi, A. Ayatollahi, and A. Mirzaei, "A wavelet-approximate entropy method for epileptic activity detection from eeg and its sub-bands," *Journal of Biomedical Science and Engineering*, vol. 3, no. 1, pp. 1182–1189, October 2010.

[45] Y. C. Liang, Z. Wu, and B. Li, "A new 12-bit fully differential sar adc for wireless implantable neural recording system," in *Electron Devices and Solid-State Circuits, 2009. EDSSC 2009. IEEE International Conference of*, 2009, pp. 399–402.

[46] P. Si, A. Hu, S. Malpas, and D. Budgett, "A frequency control method for regulating wireless power to implantable devices," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 2, no. 1, pp. 22–29, March 2008.

[47] S. A. P. Haddad and W. A. Serdijn, *Ultra Low-Power Biomedical Signal Processing*. Springer, 2009.

[48] A. Casson and E. Rodriguez-Villegas, "A 60 pw g_mC continuous wavelet transform circuit for portable eeg systems," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 6, pp. 1406–1415, 2011.

[49] Q. Ma, M. Haider, S. Yuan, and S. Islam, "Power-oscillator based high efficiency inductive power-link for transcutaneous power transmission," in *Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium on*, 2010, pp. 537–540.

[50] Q. Ma, M. Haider, and Y. Massoud, "Robust power oscillator design for inductive-power link applications," in *Electronics, Circuits and Systems (ICECS), 2011 18th IEEE International Conference on*, 2011, pp. 109–112.

[51] ——, "Power-loss reduction of a mosfet cross-coupled rectifier by employing zero-voltage switching," in *Electronics, Circuits and Systems (ICECS), 2011 18th IEEE International Conference on*, 2011, pp. 252–255.

[52] A. Mirzaei, M. Heidari, R. Bagheri, S. Chehrazi, and A. Abidi, "The quadrature lc oscillator: A complete portrait based on injection locking," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 9, pp. 1916–1932, Sept 2007.

[53] Y. Ramadass and A. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 1, pp. 189–204, Jan 2010.

[54] Q. Ma, M. Haider, and Y. Massoud, "A low-loss rectifier unit for inductive-powering of biomedical implants," in *VLSI and System-on-Chip (VLSI-SoC), 2011 IEEE/IFIP 19th International Conference on*, Oct 2011, pp. 86–89.

[55] ——, "Power-loss reduction of a mosfet cross-coupled rectifier by employing zero-voltage switching," in *Electronics, Circuits and Systems (ICECS), 2011 18th IEEE International Conference on*, Dec 2011, pp. 252–255.

[56] T. Lehmann and Y. Moghe, "On-chip active power rectifiers for biomedical applications," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, May 2005, pp. 732–735 Vol. 1.

[57] Y.-H. Lam, W.-H. Ki, and C.-Y. Tsui, "Integrated low-loss cmos active rectifier for wirelessly powered devices," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 53, no. 12, pp. 1378–1382, Dec 2006.

[58] S. Guo and H. Lee, "An efficiency-enhanced cmos rectifier with unbalanced-biased comparators for transcutaneous-powered high-current implants," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 6, pp. 1796–1804, June 2009.

[59] Y. Perelman and R. Ginosar, "An integrated system for multichannel neuronal recording with spike/lfp separation, integrated a/d conversion and threshold detection," *IEEE Transactions on Biomedical Engineering*, vol. 54, no. 1, pp. 130 –137, jan. 2007.

[60] Y.-K. Song, W. Patterson, C. Bull, J. Beals, N. Hwang, A. Deangelis, C. Lay, J. McKay, A. Nurmikko, M. Fellows, J. Simeral, J. Donoghue, and B. Connors, "Development of a chipscale integrated microelectrode/microelectronic device for brain implantable neuroengineering applications," *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 13, no. 2, pp. 220 –226, june 2005.

[61] S. Lee, S. Lee, and C. Chiang, "0.9 v low-power switched-opamp switched-capacitor bandpass filter for electroneurography acquisition systems," *Circuits, Devices Systems, IET*, vol. 2, no. 2, pp. 257–263, April 2008.

[62] P. Si, A. Hu, S. Malpas, and D. Budgett, "A frequency control method for regulating wireless power to implantable devices," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 2, no. 1, pp. 22–29, March 2008.

[63] K. G. Oweiss, A. Mason, Y. Suhail, A. Kamboh, and K. Thomson, "A scalable wavelet transform vlsi architecture for real-time signal processing in high-density intra-cortical implants," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 54, no. 6, pp. 1266–1278, June 2007.

[64] Z. Nenadic and J. Burdick, "Spike detection using the continuous wavelet transform," *Biomedical Engineering, IEEE Transactions on*, vol. 52, no. 1, pp. 74–87, Jan 2005.

[65] C. A. Mead, *Analog VLSI and Neural Systems*. Addison-Wesley, 1989.

[66] G. Indiveri, E. Chicca, and R. Douglas, "A VLSI array of low-power spiking neurons and bistable synapses with spike-timing dependernt plascity," *IEEE Transactions on Neural Networks*, vol. 7, no. 1, pp. 211–221, 1989.

[67] F. Folowsele and A. Harrison, "A switched capacitor implementaion of the generalized linear integrate-fire-neuron," in *International Symposium on Circuits and Systems*, 2009, pp. 24–27.

[68] S. M. R. Hasan and W. L. Xu, "Low-voltage analog current-mode central pattern generator circuit for robotic chewing locomotion using 130nanometer CMOS technology," in *Internatonal Conference on Microelectronics*, 2007, pp. 155–160.

[69] M. H. Thaut, G. P. Kenyon, M. L. Schauer, , and G. C. McIntosh, "The connection between rhythmicity and brain function," *IEEE Engineering in Medicine and Biology Magazine*, vol. 18, pp. 101–108, 1999.

[70] S. Ehsan and K. D. McDonald-Maier, "On-board vision processing for small UAVs: time to rethink strategy," in *ASA/ESA Conference on Adaptive Hardware and Systems*, 2009, pp. 75–81.

[71] E. J. Basham and D. W. Parent, "An analog circuit implementation of a quadratic integrate and fire neuron," in *Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, 2009, pp. 741–744.

[72] J. H. B. Wijekoon and P.Dudek, "Integrated circuit implementation of a cortical neuron," *IEEE International Symposium on Circuits and Systems*, pp. 1784–787, 2008.

[73] A. Hodgkin and A. Huxley, "A quantitative description of membrane current and its application to conduction and excitation in nerve," *J. Physiol*, vol. 117, pp. 550–554, 1952.

[74] P. Georgiou and C. Toumazou, "A silicon pancreatic beta cell for diabetes," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, pp. 39–49, 2007.

[75] M. F. Simoni, G. S. Cymbalyuk, M. E. Sorensen, R. L. Calabrese, and S. P. DeWeerth, "A multiconductance silicon neuron with biologically matched dynamics," *IEEE Transactions on Biomedical Engineering*, vol. 51, pp. 342–354, 2004.

[76] R. P. Shorten and J. N. David, "A Hodgkin-Huxley model exhibiting bursting oscillations," *Report Number: 187*, Dec. 1999.

[77] M. T. Rosenstein, J. J. Collins, and C. J. D. Luca, "A practical method for calculating largest lyapunov exponents from small data sets," *Phys. D 65*, pp. 117–134, 1993.

[78] T. Yu and G. Cauwenberghs, "Analog VLSI neuromorphic network with programmable membrane channel kinetics," *Proc. Int. Symp. Circuits Syst.*, pp. 349–352, May 2009.

[79] Q. Ma, Y.-G. Li, M. Haider, and Y. Massoud, "A low-power neuromorphic bandpass filter for biosignal processing," in *Wireless and Microwave Technology Conference (WAMICON), 2013 IEEE 14th Annual*, April 2013, pp. 1–3.

[80] Q. Ma, M. Haider, Y.-G. Li, and Y. Massoud, "A low-power neuromorphic bandpass filter for biosignal," *Processing Proceedings of the IEEE Wireless and Microwave Technology Conference*, April 2013.

[81] T. Jochum, T. Denison, and P. Wolf, "Integrated circuit ampliers for multi-electrode intracortical recording," *Journal of Neural Engineering*, vol. 6, no. 1, p. 012001, January 2009.

[82] E. Spinelli, N. Martinez, M. Mayosky, and R. Pallas-Areny, "A novel fully differential biopotential amplifier with dc suppression," *IEEE Transactions on Biomedical Engineering*, vol. 51, no. 8, pp. 1444 –1448, aug. 2004.

[83] L. Liu, X. Zou, W. Goh, R. Ramamoorthy, G. Dawe, and M. Je, "800 nw 43 nv/ $\sqrt{}$hz neural recording amplifier with enhanced noise efficiency factor," *Electronics Letters*, vol. 48, no. 9, pp. 479 –480, 26 2012.

[84] C. Liu, J. Chang, S. Yuan, L. Johnson, and R. Rennaker, "A low noise bandpass neuro-amplifier with adjustable bandwidth for bio-medical applications," in *Green Circuits and Systems (ICGCS), 2010 International Conference on*, june 2010, pp. 438 –441.

[85] V. Majidzadeh, A. Schmid, and Y. Leblebici, "Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 3, pp. 262 –271, june 2011.

[86] M. Yin and M. Ghovanloo, "A low-noise preamplifier with adjustable gain and bandwidth for biopotential recording applications," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, may 2007, pp. 321 –324.

[87] F. Shahrokhi, K. Abdelhalim, D. Serletis, P. Carlen, and R. Genov, "The 128-channel fully differential digital integrated neural recording and stimulation interface," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 3, pp. 149 –161, june 2010.

[88] B. Gosselin, M. Sawan, and C. Chapman, "A low-power integrated bioamplifier with active low-frequency suppression," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, no. 3, pp. 184 –192, sept. 2007.

[89] E. Spinelli, N. Martinez, M. Mayosky, and R. Pallas-Areny, "A novel fully differential biopotential amplifier with dc suppression," *IEEE Transactions on Biomedical Engineering*, vol. 51, no. 8, pp. 1444 –1448, aug. 2004.

[90] T. Degen and H. Jackel, "A pseudodifferential amplifier for bioelectric events with dc-offset compensation using two-wired amplifying electrodes," *IEEE Transactions on Biomedical Engineering*, vol. 53, no. 2, pp. 300 –310, feb. 2006.

[91] E. A. Vittoz, "Design of analog digital vlsi circuits for telecommunications and signal processing," *Micropower techniques*, pp. 53–96, 1994.

[92] M. Steyaert and W. Sansen, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *Solid-State Circuits, IEEE Journal of*, vol. 22, no. 6, pp. 1163–1168, 1987.

[93] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor, "Micropower cmos integrated low-noise amplification, filtering, and digitization of multimodal neuropotentials," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 3, no. 1, pp. 1–10, 2009.

[94] P. Addison, J. Walker, and R. Guido, "Time–frequency analysis of biosignals," *Engineering in Medicine and Biology Magazine, IEEE*, vol. 28, no. 5, pp. 14–29, September 2009.

[95] M. Sifuzzaman, M. Islam1, and M. Ali, "Application of wavelet transform and its advantages compared to fourier transform," *Journal of Physical Sciences*, vol. 13, pp. 121–134, October 2009.

[96] C. W. Clenshaw, “A comparison of ”best” polynomial approximations with truncated chebyshev series expansions,” *Journal of the Society for Industrial and Applied Mathematics: Series B, Numerical Analysis*, vol. 1, pp. pp. 26–37, 1964. [Online]. Available: http://www.jstor.org/stable/2949762

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